IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS & SYSTEMS

ISCAS·2017

BALTIMORE, MD, USA | MAY 28-31, 2017

from Dreams to Innovation

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ABOUT ISCAS 2017

The IEEE International Symposium on Circuits and Systems (ISCAS) is the world's largest networking forum of researchers in the highly active fields of theory, design and implementation of circuits and systems. The 2017 edition, sponsored by the IEEE Circuits and Systems Society (CASS), will be held in Baltimore, Maryland, USA, from May 28 to 31, 2017. This meeting will focus on the connection from Dreams to Innovation with the aim of cultivating creative, research-driven ideas in Circuits and Systems as they transition to Innovations and fuel economic development. The technical program has been tailored to reflect the wide spectrum of research interests and applications shared by researchers in the field. The selected topics are of particular interest to the circuits & systems community:

- Analog and Mixed Signal Circuits and Systems
- Digital Integrated Circuits and Systems
- Communications Circuits and Systems
- Power and Energy Circuits and Systems
- Beyond CMOS: Nanoelectronics and Hybrid Systems Integration
- Biomedical Circuits and Systems
- Sensory Circuits and Systems
- Neural Networks and Neuromorphic Engineering
- Nonlinear Systems and Circuit Theory
- Digital Signal Processing
- Visual Signal Processing and Communications
- Multimedia Systems and Applications
- Education in Circuits and Systems
- Internet of Video Things

ABOUT THE IEEE CIRCUITS AND SYSTEMS SOCIETY

Mission

The mission of the IEEE Circuits and Systems Society is to foster CASS members across disciplines to address humanity's grand challenges by conceiving and pioneering solutions to fundamental and applied problems in circuits and systems.

Vision

The IEEE Circuits and Systems Society (CASS) believe that the Grand Engineering Challenges of the 21st century can only be addressed in an interdisciplinary and cross-disciplinary manner. The Society's unique and profound expertise in Circuits, Systems, Signals, Modeling, Analysis, and Design can have a decisive impact on important issues such as Sustainable Energy, Bio-Health, Green Information Technology, Nano-Technology, and Scalable Information Technology Systems.

For more information, please visit our website at http://ieee-cas.org/

WELCOME MESSAGE - GENERAL CHAIRS

Pamela Abshire
University of Maryland
College Park, MD, USA

Ralph Etienne-Cummings
Johns Hopkins University
Baltimore, MD, USA

It is a great pleasure to welcome you to the 50th edition of the IEEE International Symposium on Circuits and Systems (ISCAS 2017) in Baltimore. As it has done for half a century, ISCAS brings together a vibrant, multidisciplinary community of researchers from around the world in a diverse range of technical domains encompassing the field of Circuits and Systems. This year our Conference Theme — *from Dreams to Innovation* — highlights our community's strong history of cultivating creative research that leverages the integration of theory, algorithms, design, and hardware to generate ideas that develop into inventions and innovations and fuel global economic development. While we are eager to see our familiar colleagues again, we particularly welcome all new faces to ISCAS, and we look forward to an extensive future of collaboration, discourse and innovation together.

It is fitting in this 50th edition of ISCAS that we embrace our past and also look forward to the future. In special technical sessions on Monday and Tuesday, May 29-30, we will honor distinguished delegates from the first years of ISCAS as *Pioneers of Circuits and Systems* as they share their perspectives on important technical achievements over the past 50 years and into the future. In the evening on Monday, May 29, Women in Circuits and Systems and the Young Professionals Program will host the FutureCAS Panel which will discuss trends in technology and society and what challenges and opportunities they will bring to the field of Circuits and Systems. We encourage you to attend these special events to reflect upon progress in our field and to share your insights with colleagues both familiar and new.

This year we have made a few changes to the structure of the conference in order to strengthen the technical contributions, educational content, and outreach efforts of the conference. The conference begins with a day of tutorials on Sunday, May 28, and continues with mini-tutorials which are offered during the first session on each day of the technical program. The first two days of the technical program, Monday and Tuesday May 29-30, each end with an interactive poster session in the fourth floor Ballroom. All are encouraged to grab a drink and gather around for hearty discussions and debates about the newest ideas in our field. We have

reorganized the conference track structure to be centered and streamlined around technical topics. As a consequence, duplicate sub-tracks have been consolidated and the quality of the review process has been enhanced. We hope that you will experience the benefits of this years' effort throughout ISCAS 2017. We sincerely thank the Technical Committees' leadership and the Technical Program Co-Chairs, Professors Tor (Bassen) Sverre Lande and Håkan Johansson, for working with us to make this a reality.

In addition to the realignment of the Tracks and Sub-tracks of the conference, this year we have also introduced Innovation Themes within the technical program to highlight papers on timely interdisciplinary topics. Nearly half (51 of 117) of the lecture sessions are aligned with one of these cross-cutting Innovation Themes. The Keynote Speakers have also been invited to line up with Innovation Themes on each day of the conference. Moreover, a number of invited talks from industry are integrated throughout the technical program so that ISCAS's technical contributions can be placed in context relative to their commercial and societal impact. The Innovation Themes for ISCAS 2017 are *Internet of Things*, *Cognitive Computing & Deep Learning*, *Hardware Security*, *Brain: Innovative NeuroTechnologies*, *Analog & Digital Senses*, *Autonomous Vehicles, Robotics & UAVs*, and *Smart Buildings & Cities*. Our three Keynote Speakers are Miyoung Chun (Brain) of The Kavli Foundation, Kerry Bernstein (Hardware Security) of DARPA, and Tyson Tuttle (Internet of Things) of Silicon Labs, Inc. We thank them for participating in this year's ISCAS, and the Keynote Co-Chairs, Professors Andreas Andreou, David Skellern, and Georges Gielen for their hard work in bringing them to our community.

Overall, we have been fortunate to have assembled a very dynamic and diligent Organizing Committee. Thank you all for attending the many OC meetings, for sharing your great ideas and for going the extra mile to help us organize ISCAS 2017. You are the foundation upon which this conference is built.

Thank you to Chris Dyer and the Conference Catalysts team and Tom Wehner of ePapers for all of your work behind the scenes. We sincerely thank all of the Authors, Track Chairs, Review Committee Members, Reviewers, Session Chairs, Tutorial and Special Session Organizers, and the Invited Speakers. This conference would not be possible without your contributions. We also thank the technical and financial sponsors, in particular, Johns Hopkins University and the University of Maryland, College Park, for allowing us to invest the time to organize ISCAS 2017.Finally, we thank the IEEE CAS Society for selecting us to host this edition of ISCAS in Baltimore, MD.

In this 50th ISCAS we are fortunate to visit some historic venues during our social events. ISCAS 2017 is held on the waterfront in the Inner Harbor of Baltimore, MD, adjacent to the historic Fells Point and popular Little Italy. A large number of restaurants, bars and shopping centers are located within a short walking distance of the conference venue. The welcome reception will be hosted alongside the dinosaurs at the Maryland Science Center in the Inner Harbor. The banquet will take place at Fort McHenry, one of the most important sites in early US history which gave birth to our national anthem *The Star-Spangled Banner.* We are looking forward to welcoming you all to our city and hope that you will enjoy both the technical and social aspects of the conference and that you will take away new ideas and fond memories. Happy Conferencing!!

WELCOME MESSAGE - TECHNICAL PROGRAM CHAIRS

Håkan Johansson
Linköping University, Sweden

Tor Sverre Lande
University of Oslo, Norway

As Technical Program Chairs for the 2017 IEEE International Symposium on Circuits and Systems in Baltimore, MD, USA, we have done our best to ensure an engaging technical program. Some exciting new twists to the program combined with well-established and proud traditions of ISCAS are intended to make the conference even more interesting. One important change is the introduction of Innovation Themes as an effort to bridge contributions across different technical fields. You will find tracks on *Cognitive Computing & Deep Learning*, *Internet-of-Things*, *Digital & Analog Senses*, *Hardware Security*, *Brain: Innovative NeuroTechnologies*, *Autonomous Vehicles, Robotics, & UAVs*, and *Smart Buildings & Cities* binding together papers from different technical activities. We hope these high-level themes may attract more attendees and add new cross-disciplinary perspectives to our field.

We continue the ISCAS tradition of presenting three interesting keynote speakers, each addressing one of our central Innovation Themes. On Monday Miyoung Chun, Executive VP of Science Programs of The Kavli Foundation, will give a talk on "The BRAIN Initiative: Building, Strengthening, and Sustaining" followed by a keynote talk on Tuesday by Kerry Bernstein, Program Manager at DARPA, on "A Matter of Trust". Then finally on Wednesday Tyson Tuttle, President and CEO of Silicon Labs, will give a talk on "Unleashing the Promise of the Internet of Things". In addition to keynotes we have no less than 12 invited talks touching most of our conference themes for you to enjoy.

We also continue the new ISCAS traditions of Late-Breaking News, with four sessions granting our attendees access to the latest achievements within selected fields, and presentations of abstracts from accepted papers in IEEE Circuits and Systems journals in 2016. This year we have integrated the journal abstracts into topically matched regular sessions.

It is our very special honor this year to celebrate the 50th edition of ISCAS. You will have a unique chance to meet some of the attendees of the first ISCAS in 1968 in the two "Pioneers of Circuits and Systems" sessions taking place on Monday and Tuesday afternoons. You will also find our usual Sunday tutorials, this year with three full-day tutorials and 14 half-day tutorials. We are also offering one mini-tutorial on each day of the main conference. We have prepared 113 lecture sessions and 21 poster sessions selected from 1339 submitted papers with an acceptance rate of 45.7%. In addition, we have 102 papers in special sessions and 34 exciting demonstrations for you to enjoy together with snacks and drinks. This year we received a large number of submissions from the Asia/Pacific region (35.9%) closely followed by North-America (34.1%).

We are fortunate to have a large number of dedicated reviewers for ISCAS. No less than 5788 reviews were submitted this year, giving an average of almost 4 reviews for all papers submitted to regular tracks. Without the dedicated efforts from 39 Track Chairs and 370 Review Committee Members as well as 3268 Reviewers engaged in the ISCAS review process, preparing the technical program for ISCAS in Baltimore would have been impossible! Special thanks go to Tom Wehner and his ePapers system for sustained and patient guidance. Important new functionality, like CrossCheck plagiarism checking and themes handling has made it possible to improve our technical program. At last we emphasize the importance of the engagement of the organizational committee members for continuously putting forward constructive and insightful suggestions for the technical program.

Finally, we recommend perhaps one of most important program features – which is the program breaks for you to enjoy with your friends and to help make new friends. Our venue allows for plenty of room for private discussions as well as snacks and drinks during poster and demo sessions. Please engage in and enjoy the friendly environment of the flagship conference of the IEEE Circuits and Systems Society.

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KEYNOTE SPEAKERS

MIYOUNG CHUN
Executive VP of Science Programs, The Kavli Foundation

The BRAIN Initiative: Building, Strengthening, and Sustaining

Monday, May 29th, 2017
10:00am – 11:00am
Grand Ballroom V-VI

*See page 48 in Technical Program Schedule

ABSTRACT: The BRAIN Initiative seeks to revolutionize our understanding of brain function and human behavior by bringing together diverse groups of experts to discover groundbreaking tools and methods. I would like to provide my personal experience and perspective on how the BRAIN Initiative came to be, the current status, and the future activities that will sustain the Initiative in the years to come.

BIO: Dr. Chun's career spans a wide range of experience in academia and industry. Her academic career began as an Assistant Professor of Biochemistry and a member of Whitaker Cardiovascular Institute at Boston University School of Medicine in 1995. There she taught in the areas of cell biology and molecular medicine, and conducted research in signal transduction of G-protein coupled receptors.

From 1999 to 2004 she worked for Millennium Pharmaceuticals Inc. as a scientist and project leader, where her research focused on genomics/functional genomics and on molecular imaging in drug discovery and development. She discovered and characterized novel genes that are important to inflammatory and cardiovascular diseases, and has over 30 U.S. and International issued/published patents.

In 2004 she moved back to academia as Assistant Dean of Science and Engineering at the University of California, Santa Barbara (UCSB), in particular serving the California Nanosystems Institute. She was also appointed Director of International Research Advancement at UCSB. In this role she was active in building partnerships among academia, government and industry around the globe.

Dr. Chun was Vice President of Science Programs at The Kavli Foundation since 2007 and became Executive Vice President of Science Programs in 2013.

She obtained her Ph.D. degree in Molecular Genetics from The Ohio State University in 1990 and was a Postdoctoral Fellow at MIT's Whitehead Institute studying the cell and molecular biology of receptors.

KERRY BERNSTEIN
Program Manager, Microsystems Technology Office, DARPA

A Matter of Trust

Tuesday, May 30th, 2017
9:30am – 10:30am
Grand Ballroom V-VI

*See page 94 in Technical Program Schedule

ABSTRACT: Virtually every endeavor in the human experience has been thoroughly penetrated by integrated circuit technology. Along with the unprecedented capabilities that electronics provides our civilization, it also presents new threats to our personal and national economics, security, safety, and health. The manner by which we bestow trust on the technologies through which we conduct our daily affairs has never been more important; yet we are not equipped to effectively recognize vulnerabilities. Certainly, we are too aware of recent exploits in our software and networks; but less known is that the hardware hosting these capabilities may be counterfeited or compromised. Given that the human "OS" going forward will be expressed on electronic platforms, it is imperative that we evolve our means of accurately assessing technical trustworthiness. This talk will provide an overview of the electronic threat space and some of the approaches DARPA is developing for mitigating them. Our culture's propensity for trading security and privacy for convenience and cost makes it critical that our authentication solutions be accurate, fast, easy, inexpensive, and ubiquitous.

BIO: Kerry Bernstein is a program manager in the Microsystems Technology Office at DARPA. His interests are in the area of hardware security assurance and authentication and emerging high performance post-CMOS technologies. Mr. Bernstein formerly spent 33 years at the IBM T.J. Watson Research Center and IBM Microelectronics, working in the areas of leading edge, high performance/low-power devices/circuits, and 3D Integration. He attributes any successes realized to be due in large part to being surrounded by wonderful people throughout his career. Mr. Bernstein received his B.S. (1978) in Electrical Engineering from Washington University in St. Louis, Missouri. He has co-authored four (4) textbooks, holds 155 patents, and is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE).

TYSON TUTTLE
President and CEO, Silicon Labs

Unleashing the Promise of the Internet of Things

Wednesday, May 31st, 2017
10:45am – 11:45am
Grand Ballroom V-VI

**See page 142 in Technical Program Schedule*

ABSTRACT: The Internet of Things (IoT) has been hailed as the next frontier of innovation in which the everyday "things" in our homes, offices, cars, factories and cities connect to the Internet in ways that improve our lives and transform industries. The IoT market is poised to exceed 75 billion devices by 2025, but several challenges remain in achieving the market's full potential. Tyson Tuttle, CEO and President of Silicon Labs, will explore what it will take to accelerate the promise of IoT. In his keynote, Tyson will consider the market imperatives and engineering challenges of adding connectivity to electronic devices, including cost, ease of use, energy efficiency, interoperability, future extensibility and security. Addressing these challenges will unleash the limitless possibilities of a more connected world.

BIO: Tyson Tuttle serves as the Chief Executive Officer of Silicon Labs, a leading provider of silicon, software and solutions for a smarter, more connected world. Since joining Silicon Labs in 1997, Tyson has significantly shaped the company's strategic and technological directions. He helped design Silicon Labs' first breakthrough IC product, which achieved market share leadership in PC modems and enabled the company to go public in 2000. Tyson led the marketing effort behind Silicon Labs' first RF transceiver products for mobile handsets and spearheaded the development and market success of the company's radio and TV tuner ICs. Tyson led Silicon Labs' broadcast product lines until 2010 when the R&D team was consolidated under his leadership as Chief Technology Officer. He became Chief Operating Officer in 2011, managing Silicon Labs' business units and R&D, and was promoted to CEO in 2012. In his C-level roles, Tyson spearheaded the company's focus on the Internet of Things, and drove the strategic acquisitions of Ember (the ZigBee market leader), Energy Micro (the pioneer of ultra-low-power ARM-based microcontrollers) and Bluegiga (a leading provider of Bluetooth and Wi-Fi modules and software). Tyson has more than 25 years of semiconductor experience with industry leaders like Broadcom and Cirrus Logic / Crystal Semiconductor, holds 70 patents in RF and mixed-signal IC design, and serves on the board of the Global Semiconductor Alliance. Tyson holds a BS in electrical engineering from Johns Hopkins University and an MS in electrical engineering from UCLA. He is also a respected leader in the Austin community, serving on the board of directors of KUT-FM and KLRU-TV, home of PBS and Austin City Limits.

PIONEERS OF CAS SESSIONS

This year we celebrate the 50th edition of ISCAS. What is now the preeminent annual forum for a vibrant, multidisciplinary community of circuits and systems researchers from around the world began in 1968 as a small gathering of distinguished circuit theorists in Miami Beach, Florida. Omar Wing of Columbia University served as General Chair, and Bharat Kinariwala of the University of Hawai'i was the Technical Program Chair. While it was initially called the International Symposium on Circuit Theory, it has been known as the International Symposium on Circuits and Systems since the 1974 edition. For 50 years, ISCAS has played a central role in promoting technical exchange and progress within the field of Circuits and Systems.

In two special Pioneers of Circuits and Systems sessions on Monday, May 29, and Tuesday, May 30, we are fortunate to honor distinguished delegates from the first years of ISCAS as they share their perspectives on important technical achievements over the past 50 years and into the future.

**See pages 85 and 133 in Technical Program Schedule*

FUTURECAS PANEL

What challenges and opportunities does the future hold for the field of Circuits and Systems?

Monday, May 29th
Time: 6:00pm - 7:30pm
Room: Grand Ballroom V-VI

Sponsored by the Women in Circuits and Systems and the Young Professionals Program of the IEEE Circuits and Systems Society

Moderator:
Jennifer Blain Christen, Arizona State University, USA

Panelists:
Jeannette M. Wing, Corporate Vice President, Microsoft Research, USA
Orla Feely, Vice President for Research, University College Dublin, Ireland
Mandy Pant, Academic Research Director at Intel, USA
Frederica Darema, Director of Air Force Office of Scientific Research, USA

OVERVIEW: Electronics, circuits and systems have facilitated enormous technological progress in society over recent decades. Electronics has enabled many new applications spanning from aerospace devices to ubiquitous communications to personal health. So far, most of the progress in circuit design and electronics has been driven by material science - we have progressively moved to more miniature and ultra low power circuit components. However, this steady growth cannot continue forever due to fundamental physical limits that we are beginning to approach. The electronics industry will eventually see the end of its CMOS road-map. Will this make circuit design obsolete? Or will this spur us to find a new paradigm for our field?

The field of circuits and systems faces inevitable changes. How are we, as a research community, going to respond? What will that mean for the individuals who are the practitioners of our field, whether they are in academia, industry, or government labs? The field of Circuits and systems integrates knowledge on system design, engineering, mathematics and physics. Will we be able to put these together and provide our own drivers for further development?

- What are the new challenges facing society, industry and academia?
- How can we, as a research community, best response to these challenges?
- How do we facilitate collaboration between industry and academia?
- How should we educate the next generation of multidisciplinary engineers?

**See page 85 in Technical Program Schedule*

Join us for a reception following the panel in the Grand Ballroom Foyer.

CASS TRANSACTIONS PAPERS

We continue the new ISCAS tradition, started in 2016, of inviting authors of papers in the following journals (co)sponsored by the IEEE Circuits and Systems Society to present their papers at ISCAS 2017. Eligible papers were published (or in the prepublication list) between January 1, 2016 and December 31, 2016. This year we are proud to feature 73 of these papers (70% acceptance rate) alongside contributed papers in topically aligned technical sessions.

- IEEE Transactions on Circuits and Systems – Part I: Regular Paper
- IEEE Transactions on Circuits and Systems – Part II: Express Briefs
- IEEE Transactions on Circuits and Systems for Video Technology
- IEEE Transactions on Biomedical Circuits and Systems
- IEEE Transactions on Very Large Scale Integration (VLSI) Systems
- IEEE Transactions on Multimedia
- IEEE Design & Test

LIVE DEMONSTRATIONS

We continue the longstanding tradition of featuring Live Demonstrations of Circuits and Systems at ISCAS 2017. This track offers an interactive and tangible form of presentation, in which presenters have the opportunity to show working proof of their systems. The demo sessions will feature 34 live demonstrations to be held in the Harborside Ballroom on both Monday and Tuesday afternoons. The demo sessions will be presented as an extended session, starting at the same time as the afternoon technical sessions and continuing alongside the poster sessions. Please join us at the sessions and have an enjoyable first-hand experience with the demonstrations as you interact with, play with, and challenge them.

**See pages 68 and 114 in Technical Program Schedule*

IOVT PANEL

Deep Learning for Internet of Video Things – Hype or Hope?

Tuesday, May 30th
Time: 8:00am – 9:30am
Room: Dover BC

ABSTRACT: Internet of video things can collect a massive amount of video data. If the contents are properly analyzed, a great amount of information and commercial value can be extracted. To minimize human involvement, many people have high hopes for using deep learning. This is because deep learning has demonstrated the possibility of solving many difficult problems in recent years. In this panel, experts working on different areas will share their views about the collected vision of deep learning for Internet of Video Things.

Some panelists will explain why the optimism might be overly simplified and the enthusiasm might be exaggerated. For example, doubt abounds about the limitations of deep learning, in terms of the amount of computation on the edge devices, the amount of bandwidth to the cloud, and the accuracy in real world applications. Meanwhile, some panelists will provide evidence showing the significant progress in addressing the challenges, e.g., innovative devices/circuits for low-power machine intelligence, new wireless communication protocols/circuits for higher bandwidth and shorter latency, new video compression/summarization technologies to reduce communication requirements, etc.

Is deep learning for the Internet of Video Things hype or hope? You will judge.

Moderators:
Dr. Yen-Kuang Chen, Intel Corporation, USA
Prof. Eduard Alarcon, UPC, Spain

Panelists:
Prof. Magdy Bayoumi, University of Louisiana at Lafayette, USA
Prof. Shao-Yi Chien, National Taiwan University, Taiwan
Dr. Shipeng Li, Cogobuy/IngDan, China
Prof. Yung-Hsiang Lu, Purdue University, USA
Prof. Tokunbo Ogunfunmi, Santa Clara University, USA

**See page 86 in Technical Program Schedule*

PITCH YOUR STARTUP

The ISCAS "Pitch Your Startup" competition returns in 2017! This special session aims to promote industry participation and entrepreneurship by showcasing new ventures resulting from research in the CAS community. We are having this event at the beginning of ISCAS to encourage entrepreneurially-minded members of CAS to meet and to continue discussions throughout the conference. This competition is open to all startups with at least one member (student or regular) in CASS. Each speaker will have 5 minutes to present his or her company, followed by a short Q&A. Three awards will be given: an Innovation Prize for the venture showcasing the best technical innovation, a Humanitarian Prize for the venture most likely to improve the human condition, and a People's Choice award. The first two awards will be chosen by a special jury, while the third award will be chosen by audience vote. We invite you to attend this special session to encourage these promising companies and give them your valuable feedback. We also hope this session allows you to meet fellow entrepreneurs you might not otherwise meet in the regular sessions.

*See page 42 in Technical Program Schedule

CASS STUDENT DESIGN COMPETITION

ISCAS 2017 is proud to host the First IEEE Circuits and Systems Society Student Design Competition, sponsored by the Regional and Membership Activities Division of the CASS Board of Governors. The CASS Student Design Competition is a worldwide competition in which undergraduate students team with high school students to envision and engineer projects with the goal of encouraging High School Students to study Electrical Engineering and related areas. Each project will develop a solution to a real-life problem based on circuits and systems. The first and second phases of the competition were conducted at the Chapter and Regional levels. The final international phase of the competition will take place during the afternoon technical session phase on Monday, May 29, 2017. The finalists will present their projects in the live demonstration session in the Harborside Ballroom on the afternoon of Tuesday, May 30. Winners will be announced during the awards ceremony on Wednesday, May 31.

*See page 67 in Technical Program Schedule

LATE BREAKING NEWS

The world of Circuits and Systems is rapidly changing as designers battle with the end of Moore's law, the push toward both dense and distributed systems, and an increasingly complex world with increasing user transparency. In response to the fast pace of changes, ISCAS added a new track in 2016 called Late Breaking News. Late Breaking News (LBN) is a venue for fast dissemination of novel, high impact results in all topical areas spanning the technical breadth of CASS, including cross-cutting topics and those that reach beyond disciplines traditionally represented at ISCAS. LBN authors submitted contributions to a post-deadline call, which were subjected to a thorough review process selecting those of highest quality and significance (31% acceptance rate). These papers will be presented in four special sessions and featured in a special Issue of the Transactions on Circuits and Systems II.

POSTER SESSIONS

The first two days of the technical program, Monday and Tuesday May 29-30, each end with an interactive poster session in the 4th floor Harborside Ballroom. All delegates are encouraged to grab a drink and gather around for hearty discussions and debates about the newest ideas in our field.

Guide to Poster Numbering:

The prefix letter below can be seen in the program listing and will be followed by the sequential poster number for that day. Please check the poster layout outside of the Harborside Ballroom for the specific poster locations.

MONDAY POSTER SESSION

O: Demonstration Session I/Sensory Systems
P: Biomedical Signal Processing
Q: Optimization and Manufacturability
R: Communication Methods
S: Video Signal Processing & Coding Algorithms
T: Complex Networks & Models
U: Data Converters II
V: Amplifiers, Analog Filtering, RF Circuits & Interface Circuits
W: Power & Energy Modeling, Analysis, and Design

TUESDAY POSTER SESSION

O: Demonstration Session II/Integrated Biomedical Systems & BioMEMS
P: Other Areas in Analog & Mixed Signal Circuits & Systems
Q: DSP: Algorithms and Implementations
R: Nanoelectonics & Memristor Technology
S: Spiking and Learning Systems
T: Signal Processing for Interaction & Augmented Reality
U: Digital Integrated Circuits and Systems
V: Communications Security
W: Power Transfer & Charging Circuits

*See pages 71 and 117 in Technical Program Schedule

SOCIAL PROGRAM

Hand Dance Tutorial

Date: Sunday, May 28th
Time: 5:00pm - 6:00pm
Location: Grand Ballroom X

On Sunday evening from 5-6pm, we will feature a tutorial on hand dance presented by the National Hand Dance Association, whose mission of NHDA is to *Preserve, Educate and Promote the cultural art form of Hand Dance.* DC Hand Dance is a contemporary swing style partner dance with over a fifty year history as a folk and traditional art form indigenous to the Washington, DC area. It has been designated as the "Official Dance of the Nation's Capitol" by Resolution of the DC Council.

Welcome Reception

Date: Sunday, May 28th
Time: 6:30pm - 8:30pm
Location: Maryland Science Center
Address: 601 Light St, Baltimore, MD, 21230

The ISCAS 2017 Welcome Reception will be held on Sunday, May 28th from 6:30-8:30 at the Maryland Science Center. Attendees can travel from the Baltimore Marriott Waterfront easily by water taxi or by foot.

The Maryland Academy of Sciences is Maryland's oldest scientific institution and one of the oldest such institutions in the entire nation.

At its inception in 1797, the Academy was an amateur scientific society—members met to discuss papers on astronomy, botany, zoology, and other subjects then known as the "natural sciences."

A major expansion and renovation of the entire facility was completed in May of 2004. New exhibitions were added on all levels as well as the addition of a permanent hall showcasing dinosaurs and earth sciences, and a dedicated gallery for housing temporary exhibitions.

Conference Lunches

Date: Sunday, May 28th
Time: 12:30pm - 1:30pm
Location: Grand Ballroom V

We are delighted to invite all participants to enjoy a midday break for lunch to be located in Grand Ballroom 5. Volunteers will direct you to the lunch venue starting at 12:30pm.

Date: Monday, May 29th
Time: 1:00pm - 2:00pm
Location: Grand Ballroom V-VI

We are delighted to invite all participants to enjoy a midday break for lunch to be located in Grand Ballroom V-VI. Volunteers will direct you to the lunch venue starting at 1:00pm.

Date: Tuesday, May 30th
Time: 12:30pm - 1:30pm
Location: Grand Ballroom V-VI

We are delighted to invite all participants to enjoy a midday break for lunch to be located in Grand Ballroom V-VI. Volunteers will direct you to the lunch venue starting at 12:30pm.

Date: Wednesday, May 31st
Time: 11:45pm - 1:30pm

Lunch on own.

Women in Circuits and Systems/Young Professionals Reception

Date: Monday, May 29th
Time: 7:30pm – 8:45pm
Location: Grand Ballroom Foyer

The ISCAS 2017 WiCAS/Young Professionals Reception will be held on Monday, May 29th from 7:30 - 8:45 at the Baltimore Marriott Waterfront, immediately following the FutureCAS Panel.Women in Circuits and Systems (WiCAS) supports career development for IEEE CASS members, particularly women, minorities, and those at early career stages. WiCAS is a subcommittee of the Board of Governors of the IEEE Circuits and Systems Society, one of the largest and oldest of IEEE's technical societies. For more information email WiCAS Chair, Elena Blokhina (elena.blokhina@ucd.ie).

IEEE CASS Young Professionals (YP) is an international community of enthusiastic, dynamic, and innovative members and volunteers. Our YP Program works with the IEEE YP group that commits itself to helping young professionals evaluate their career goals, polish their professional image, and create the building blocks of a lifelong and diverse professional network. For more information email CASS Vice President of Regional and Membership Activities Eduardo da Silva (eabsilva@ieee.org).

Gala Dinner

Date: Tuesday, May 30th
Time: 6:30pm – 10:30pm
Location: Ft. McHenry
Address: 2400 E Fort Ave, Baltimore, MD, 21230

The ISCAS 2017 Conference Dinner will be held on Tuesday, May 30th from 6:30-10:30 at historic Ft. McHenry. Coach transportation will be provided from the Baltimore Marriott Waterfront.

Farewell Reception

Date: Wednesday, May 31st
Time: 5:30pm – 7:30pm
Location: PowerPlant Live!
Address: 34 Market Pl, Baltimore, MD, 21202

The ISCAS 2017 Farewell Reception will be held on Wednesday, May 31st from 5:30 - 7:30 at Baltimore's PowerPlant Live!, just a short 0.5 mile walk from the Baltimore Marriott Waterfront.

*Transportation will not be provided by the conference

IBUKA AWARD

2017 IEEE MASARU IBUKA CONSUMER ELECTRONICS AWARD
Sponsored by Sony Corporation

JOHN O' SULLIVAN, DAVID SKELLERN, AND TERENCE PERCIVAL
For pioneering contributions to high-speed wireless LAN technology

The efforts of John O'Sullivan, David Skellern, and Terence Percival in developing and commercializing high-speed Wi-Fi provided the milestone technology for practically all in-home and local area mobile Internet communications. O'Sullivan initiated and led the early efforts in techniques for very high-speed wireless networks at Australia's Commonwealth Scientific and Industrial Research Organization (CSIRO). Percival took over and led the CSIRO project that modeled and prototyped the high-speed modulation schemes and hardware needed for successful Wi-Fi communications. Working in conjunction with CSIRO, Skellern led a pioneering project on wireless local area networks at Macquarie University and in 1997 co-founded, with Percival and Neil Weste, Radiata Communications to commercialize the CSIRO-Macquarie research. O'Sullivan joined Radiata in 1999. In 2000 Radiata demonstrated the first working Wi-Fi system based on the IEEE 802.11a 5-GHz standard.

An IEEE Senior Member, O'Sullivan is a physicist and electrical engineer (retired). An IEEE Life Fellow, Skellern is chairman of CMCRC Ltd, Sydney, Australia. Percival is an electrical engineer and director of TMPP Pty Ltd, Northbridge, Australia.

2017 CIRCUITS AND SYSTEMS SOCIETY AWARD RECIPIENTS

Mac Van Valkenburg Award
Keshab K. Parhi
For pioneering contributions to VLSI digital signal processing architectures, design methodologies, and their applications to wired and wireless communications, and service to IEEE Circuits and Systems Society.

Charles A. Desoer Technical Achievement Award
Krishnendu Chakrabarty
For groundbreaking contributions to the design of microfluidic biochips, testing and design-for-test of system-on-chip and 3D integrated circuits, and infrastructure optimization of wireless sensor networks, as well as for extraordinary technical leadership, industry impact, and inspiring a community of researchers worldwide.

John Choma Education Award
Behzad Razavi
For his seminal books and his global impact on circuits education.

Vitold Belevitch Circuits and Systems Award
Irwin W. Sandberg
For fundamental contributions to the understanding and analysis of nonlinear circuits and systems.

Guillemin-Cauer Best Paper Award
Weisheng Zhao, Mathieu Moreau, Erya Deng, Yue Zhang, Jean-Michel Portal, Jacques-Olivier Klein, and Marc Bocquet
"Synchronous Non-Volatile Logic Gate Design Based on Resistive Switching Memories," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 2, pp. 443-454, February 2014

Darlington Best Paper Award
Bo Zhao, Nai-Chung Kuo, and Ali M. Nikne
"An Inductive-Coupling Blocker Rejection Technique for Miniature RFID Tag," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 8, pp. 1305-1315, August 2016

Biomedical Circuits and Systems Best Paper Award
Ruslana Shulyzki, Karim Abdelhalim, Arezu Bagheri, M. Tariqus Salam, Carlos M. Florez, Jose Luis Perez Velazquez, Peter L. Carlen, and Roman Genov
"320-Channel Active Probe for High-Resolution Neuromonitoring and Responsive Neurostimulation," IEEE Transactions on Biomedical Circuits and Systems, vol. 9, no. 1, pp. 34-49, February 2015

2017 CIRCUITS AND SYSTEMS SOCIETY AWARD RECIPIENTS CONTINUED

Circuits and Systems for Video Technology Best Paper Award
Thiow Keng Tan, Rajitha Weerakkody, Marta Mrak, Naeem Ramzan, Vittorio Baroncini, Jens-Rainer Ohm, and Gary J. Sullivan
"Video Quality Evaluation Methodology and Verification Testing of HEVC Compression Performance," IEEE Transactions on Circuits and Systems for Video Technology, vol. 26, no. 1, pp. 76-90, January 2016

Very Large Scale Integration Systems Best Paper Award
Yingjie Lao and Keshab K. Parhi
"Obfuscating DSP Circuits via High-Level Transformations," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 5, pp. 819-830, May 2015

Outstanding Young Author Award
Yan Lu, Yipeng Wang, Quan Pan, et al.
"A Fully-Integrated Low-Dropout Regulator with Full-Spectrum Power Supply Rejection," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 3, pp. 707-716, March 2015

Pre-Doctoral Scholarships
Divya Pathak, Drexel University, Philadelphia, Pennsylvania, USA
Xinfei Guo, University of Virginia, Charlottesville, Virginia, USA

World Chapter of the Year Award
Malaysia
Chapter Chair, Nurul Amziah Md Yunus

Region 1-7 Chapter of the Year Award
Houston
Chapter Chair, Joseph Cavallaro

Region 9 Chapter of the Year Award
Rio Grande do Sul
Chapter Chair, Ricardo Reis

Region 10 Chapter of the Year Award
Seoul
Chapter Chair, Myung Hoon Sunwoo

2017 CIRCUITS AND SYSTEMS SOCIETY NEWLY ELEVATED FELLOWS

Yu Cao
Arizona State University
Tempe, AZ, USA
For development of predictive technology models for reliable circuit and system integration

Lap-Pui Chau
Nanyang Technological University
Singapore, Singapore
For contributions to fast computation algorithms for visual signal processing

Kiyoung Choi
Seoul National University
Seoul, Korea
For contribution to low-power, real-time, and reconfigurable systems

Sorin Cotofana
Delft University of Technology
Delft, Netherlands
For contributions to nanocomputing architectures and paradigms

Ricardo De Queiroz
Universidade de Brasilia
Brasilia, Brazil
For contributions to image and video signal enhancement and compression

Michael Gard
The Charles Machine Works
Perry, OK, USA
For contributions to instrumentation-and measurement technology for petroleum exploration, computed tomography, and underground construction

Payam Heydari
University of California, Irvine
Irvine, CA, USA
For contributions to silicon-based millimeter-wave integrated circuits and systems

Kenji Itoh
Kanazawa Institute of Technology
Nonoichi, Ishikawa, Japan
For contributions to microwave harmonic mixers and applications to mobile terminal devices

Juri Jatskevich
University of British Columbia
Vancouver, BC, Canada
For contributions to modeling of electric machines and switching converters

Kuen-Jong Lee
National Cheng-Kung University
Tainan, Taiwan
For contributions to low-cost testing of digital VLSI circuits

Xin Li
Carnegie Mellon University
Pittsburgh, PA, USA
For contributions to modeling, analysis, and optimization of variability of integrated circuits and systems

Donald Y. Lie
Texas Tech University
Lubbock, TX, USA
For contributions to high linearity and high efficiency silicon RF power amplifiers for broadband wireless applications

Enrico Magli
Politecnico di Torino
Milano, Italy
For contributions to compression and communication of remotely sensed imagery

Junichi Nakamura
Brillnics Japan Inc.
Tokyo, Japan
For leadership in CMOS image sensors

Panos Nasiopoulos
University of British Columbia
Vancouver, BC, Canada
For leadership in DVD authoring and digital multimedia technologies

Borivoje Nikolic
University of California, Berkeley
Berkeley, CA, USA
For contributions to energy-efficient design of digital and mixed-signal circuits

Phillip Pace
Naval Postgraduate School
Monterey, CA, USA
For leadership in radar signal processing, receiver design, and direction finding architectures

Salvatore Pennisi
University of Catania
Catania, Italy
For contributions to multistage CMOS operational amplifiers

Weiping Shi
Texas A&M University
College Station, TX, USA
For contributions to modeling and design of VLSI interconnects

Youngsoo Shin
Korea Advanced Institute of Science & Technology
Daejeon, Korea
For contributions to design tools for low power, high speed VLSI circuits and systems

Andrei Vladimirescu
Berkeley Wireless Research Center
Berkeley, CA, USA
For contributions to the development and commercial adoption of SPICE circuit simulation

Zhihua Wang
Tsinghua University
Beijing, China
For contributions to circuits and microsystems for medical

Ying Wu
Northwestern University
Evanston, IL, USA
For contributions to motion analysis and pattern discovery in computer vision

Shuicheng Yan
Qihoo/ 360 Company
Beijing, China
For contributions to subspace learning and visual classification

Ce Zhu
University of Electronic Science & Technology
Sichuan, China
For contributions to video coding and communications

2016 CIRCUITS AND SYSTEMS SOCIETY SENIOR MEMBER ELEVATIONS

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Chris Abel
Pamela Ann Abshire
Arash Ahmadi
Ahmed Ali
Costas Argyrides
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Adrijan Baric
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ABOUT BALTIMORE AND THE VENUE

Baltimore - the colorful, diverse city that is Maryland's largest city and economic hub, is known for its beautiful harbor; quirky, distinct neighborhoods; unique museums and the world-renowned Johns Hopkins Hospital to the east and the University of Maryland Medical Center to the west.

Baltimore's Inner Harbor is a hub of activity. In just a few city blocks, you can unearth dinosaurs at the Maryland Science Center, get a history lesson at the Reginald F. Lewis Museum of Maryland African American History & Culture, pay respect to pop culture at Geppi's Entertainment Museum, or submerge yourself in exotic sea life at the National Aquarium. Other attractions include the American Visionary Art Museum, the Babe Ruth Museum, and the Port Discovery Children's Museum.

Think you're done? Not even close! Baltimore's Inner Harbor has loads of restaurants, pubs, hotels and shops, many of them at the popular Harborplace shopping and entertainment center. The Water Taxi will take you from the harbor to surrounding neighborhoods, and the free Charm City Circulator provides daily bus service through several downtown routes.

Hotel
Here at the Baltimore Marriott Waterfront, we invite you to discover waterfront relaxation in the heart of Baltimore. We boast spacious, tastefully designed hotel rooms and an extensive array of first-class amenities, as well as a terrific hotel location in downtown's bustling Harbor East district, just steps from top-quality shopping and dining.

Currency
All transactions are in US dollars. The dollar is divided into 100 cents. There are 4 coins denominated in 1, 5, 10, and 25 cents. Paper currency can be found in the following denominations: $1, $5, $10, $20, $50, $100.

Language
The official language in Baltimore is English.

Time Zone
The city of Baltimore is in the Eastern Daylight Time (EDT) zone and is 4 hours behind Coordinated Universal Time (UTC − 4)

TUTORIALS – SUNDAY, MAY 28TH

Important note: All morning tutorials start at 9:00am and end at 12:30pm, with a 30 minute coffee break at 10:30am. All afternoon tutorials start at 1:30pm and end at 5:00pm, with a 30 minute coffee break at 3:00pm.

Morning half-day tutorials | 9:00am – 12:30pm

Room: Dover A
Silicon Physical Unclonable Functions: Past, Up-to-date, and Future
Chip-Hong Chang, Nanyang Technological University, Singapore; Gang Qu, University of Maryland at College Park, USA

Room: Dover BC
Bio/Nano/CMOS interfaces for Remote Monitoring of Human Metabolism
Sandro Carrara, EPFL - Ecole Polytechnique Federale de Lausanne, Switzerland

Room: Grand Ballroom I
Soft Wireless Bioelectronics and Signal Processing for Hacking Nervous System: Opportunities and Challenges
Byung-Jun Yoon and Sung Il Park, Texas A&M University, USA

Room: Grand Ballroom II
Emerging Low-Power Wireless IoT Standards: Challenges and Trends
Danielle Griffith, Texas Instruments, USA

Room: Grand Ballroom III
Young Professionals Program Event: Aspiring PI Grantsmanship
Jennifer Blain Christen, Arizona State University, USA; Wendy Nilsen, National Science Foundation, USA

Room: Grand Ballroom IV
Compressive Sensing: Theory, Applications and Implementation of Secure Nodes for Internet of Things
Riccardo Rovatti, University of Bologna, Italy; Gianluca Setti, University of Ferrara, Italy

Room: Grand Ballroom VII
RF circuit design for the systems designer
Alyssa B. Apsel, Cornell University, USA

TUTORIALS – SUNDAY MAY 28th

Afternoon half-day tutorials | 1:30pm – 5:00pm

Room: Dover A
Neural Interface Circuits and Systems
Ross M. Walker, University of Utah, USA

Room: Dover BC
Battery Charging System and Circuit Fundamentals for Portable and IoT Devices
Ayman Fayed, The Ohio State University, USA

Room: Grand Ballroom I
Managing technology professionals: Transitioning from individual contributor to management
Tuna B. Tarim, Texas Instruments, Inc., USA

Room: Grand Ballroom II
Clock recovery Techniques
Eric Naviasky, Cadence, USA

Room: Grand Ballroom III
Cognitive Computer Architecture for Machine Learning, Data Center Processing and Internet of Things
Andreas G. Andreou, Johns Hopkins University, USA

Room: Grand Ballroom IV
Modeling and design of ultra-low-voltage circuits for energy harvesting applications
Carlos Galup Montoro and Márcio Cherem Schneider, Federal University of Santa Catarina, Brazil

Room: Grand Ballroom VII
Hardware Security: PUF Based Authentication and Functional Obfuscation
Keshab K. Parhi and Chris H. Kim, University of Minnesota, USA

Room: TBD – Check at Registration Counter
High School Maker Workshop: Interactive Jewelry

TUTORIALS – SUNDAY MAY 28th

Full-day tutorials | 9:00am – 5:00pm
Full-day tutorials follow the same schedule as half-day tutorials

Room: Grand Ballroom VIII
Memristive devices, circuits, systems and applications
Themis Prodromakis, University of Southampton, UK; Daniele Ielmini, Politecnico di Milano, Italy

Room: Grand Ballroom IX
IC Power Management Circuits and Systems with emphasis for portable devices
Edgar Sanchez-Sinencio and Jose Silva-Martinez, Texas A&M University, USA

Room: Grand Ballroom X
Algorithms and hardware architectures for data intensive computing: machine and deep learning, statistical inference
Saeid Nooshbadi, Michigan Tech, USA

Hand Dance tutorial | 5:00pm – 6:00pm
Room: Grand Ballroom X
National Hand Dance Association

Mini Tutorials

Monday, May 29th
Room: Essex AB
Memristor-CMOS hybrid circuits and systems for brain-inspired computing
Kyeong-Sik Min, Kookmin University, Korea; Fernando Corinto, Politecnico di Torino, Italy

Tuesday, May 30th
Room: Essex AB
Multiply and Filter: An Universal Measurement Trick
Arijit Sinharay, Tata Consultancy, India

Wednesday, May 31st
Room: Essex AB
Dynamic Comparator Noise and Metastability Simulation Techniques
William Evans, Cadence, USA

CMOS-bio Interfaces: Recent Trends & Future Perspectives

Time: Monday, May 29 (8:00-9:30)
Room: Dover A
Chair(s): Jens Anders - Universität Ulm; Donhee Ham - Harvard University

8:00 ***CMOS-Nano-Bio Interface Array for Cardiac and Neuro Technology***
Jeffrey Abbott, Tianyang Ye, Ling Qin, Marsela Jorgolli, Rona Gertner, Donhee Ham, Hongkun Park
Harvard University, United States

8:18 ***CMOS Bioelectronics: Emerging Application in Molecular Diagnostics, Microbiology, and Neuroscience***
Kenneth Shepard
Columbia University, United States

8:36 ***Towards CMOS-Based in-Vivo NMR Spectroscopy and Microscopy***
Jonas Handwerker{2}, Marlon Pérez-Rodas{1}, Maurits Ortmanns{2}, Klaus Scheffler{1}, Jens Anders{2}
{1}Max Planck Institute for Biological Cybernetics, Germany; {2}Universität Ulm, Germany

8:54 ***Wide-Range Optical CMOS-Based Diagnostics***
Mohammed Al-Rawhani, Boon Chong Cheah, Christos Giagkoulovits, Abdu Shakoor, Bence Nagy, James Beeley, David Cumming
University of Glasgow, United Kingdom

9:12 ***INVITED: Technology Trends and Commercialization of High-Density Microelectrode Arrays for Advanced in-Vitro Electrophysiology***
Urs Frey{2}, Marie E. Obien{2}, Jan Müller{2}, Andreas Hierlemann{1}
{1}Eidgenössische Technische Hochschule Zürich, Switzerland; {2}MaxWell Biosystems AG / Eidgenössische Technische Hochschule Zürich, Switzerland

Neuromorphic & Learning Circuits & Systems

Time: Monday, May 29 (8:00-9:30)
Room: Grand Ballroom I
Chair(s): Scott Koziol - Baylor University; Shih-Chii Liu - Swiss Federal Institute of Technology in Zurich

8:00 ***Oscillation-Based Slime Mould Electronic Circuit Model for Maze-Solving Computations***
Vasileios Ntinas{1}, Georgios Ch. Sirakoulis{1}, Ioannis Vourkas{1}, Andrew Adamatzky{2}
{1}Democritus University of Thrace, Greece; {2}University of the West of England, United Kingdom

8:18 ***Randomized Unregulated Step Descent for Limited Precision Synaptic Elements***
Lorenz Müller, Manu Nair, Giacomo Indiveri
Universität Zürich / Eidgenössische Technische Hochschule Zürich, Switzerland

8:36 ***Ultra-Low-Energy Mixed-Signal IC Implementing Encoded Neural Networks***
Benoit Larras{2}, Cyril Lahuec{1}, Fabrice Seguin{1}, Matthieu Arzel{1}
{1}TELECOM Bretagne, France; {2}Université Lille 1 / Université de Valenciennes, France

8:54 ***A Fully-Synthesized 20-Gate Digital Spike-Based Synapse with Embedded Online Learning***
Charlotte Frenkel{2}, Giacomo Indiveri{1}, Jean-Didier Legat{2}, David Bol{2}
{1}Universität Zürich / Eidgenössische Technische Hochschule Zürich, Switzerland; {2}Université Catholique de Louvain, Belgium

9:12 ***Learning in Silicon Beyond STDP: a Neuromorphic Implementation of Multi-Factor Synaptic Plasticity with Calcium-Based Dynamics***
Frank Maldonado Huayaney, Stephen Nease, Elisabetta Chicca
Universität Bielefeld, Germany

Computing with Memory Devices
Time: Monday, May 29 (8:00-9:30)
Room: Grand Ballroom II
Chair(s): Pierre-Emmanuel Gaillardon - University of Utah; Daniele Ielmini - Politecnico di Milano

8:00 ***Circuit Designs of High-Performance and Low-Power RRAM-Based Multiplexers Based on 4T(ransistor)1R(RAM) Programming Structure***
Xifan Tang{1}, Giovanni De Micheli{1}, Edouard Giacomin{2}, Pierre-Emmanuel Gaillardon{2}
{1}École Polytechnique Fédérale de Lausanne, Switzerland; {2}University of Utah, United States

8:18 ***Neuromorphic Devices and Architectures for Next-Generation Cognitive Computing***
Geoffrey W. Burr{1}, Pritish Narayanan{1}, Robert M. Shelby{1}, Stefano Ambrogio{1}, Hsinyu Tsai{1}, Scott L. Lewis{2}, Kohji Hosokawa{3}
{1}IBM Research, United States; {2}IBM T. J. Watson Research Center, United States; {3}IBM Tokyo Research Laboratory, Japan

8:36 ***RM3 Based Logic Synthesis***
Mathias Soeken{1}, Pierre-Emmanuel Gaillardon{2}, Giovanni De Micheli{1}
{1}École Polytechnique Fédérale de Lausanne, Switzerland; {2}University of Utah, United States

8:54 ***Local Memory and Logic Arrangement for Ultra-Low Power Array Processors***
Ari Paasio
University of Turku, Finland

Pitch Your Startup
Time: Monday, May 29 (8:00-9:30)
Room: Grand Ballroom III
Chair(s): Geoff Barrows - Centeye; Gabriele Manganaro – Analog Devices

Participants TBD

Interface Circuits
Time: Monday, May 29 (8:00-9:30)
Room: Grand Ballroom IV
Chair(s): Shahriar Mirabbasi - University of British Columbia; Degang Chen - Iowa State University

8:00 ***A Novel 3-Tap Adaptive Feed Forward Equalizer for High Speed Wireline Receivers***
Raga Lasya Munagala, Vijay U K
Intel Technology India Pvt Ltd., India

8:18 ***A 40 Gb/s 74.9 mW PAM4 Receiver with Novel Clock and Data Recovery***
Liangxiao Tang, Weixin Gai, Linqi Shi, Xiao Xiang
Peking University, China

8:36 ***Current Mode 1.2-Gbps SLVS Transceiver for Readout Front-End ASIC***
Hugo Hernandez, Dionisio Carvalho, Bruno Sanches, Lucas C. Severo, Wilhelmus Van Noije
Universidade de São Paulo, Brazil

8:54 ***A 10-Bit Linearity Current-Controlled Ring Oscillator with Rolling Regulation for Smart Sensing***
Michele Dei{1}, Jordi Sacristán{1}, Eloi Marigó{2}, Mohanraj Soundara{2}, Lluís Terés{1}, Francisco Serra-Graells{1}
{1}Consejo Superior de Investigaciones Científicas, Spain; {2}Silterra Malaysia Sdn. Bhd., Malaysia

9:12 ***A Low-Noise Fully-Differential Open-Loop Interface for High-G Capacitive Micro-Accelerometers with 112.2 dB Dynamic Range***
Meng Zhao, Zhongjian Chen, Zhaofeng Huang, Guangyi Chen, Wengao Lu, Yacong Zhang
Peking University, China

Video: Recording, Streaming, Synopsis, Evaluation & 3D
Time: Monday, May 29 (8:00-9:30)
Room: Grand Ballroom VII
Chair(s): Chris Lee - National Cheng Kung University

8:00 ***A Low-Power Video Recording System with Multiple Operation Modes for H.264 and Light-Weight Compression***
Hyun Kim{2}, Hyuk-Jae Lee{2}, Chae Eun Rhee{1}
{1}Inha University, Korea, South; {2}Seoul National University, Korea, South

8:18 ***Peer-Assisted Video Streaming with RTMFP Flash Player: a Measurement Study on PPTV***
Shan Zhou, Qiang Wang, Junqiang Ge, Ye Tian
University of Science and Technology of China, China

8:36 ***Multicamera Joint Video Synopsis***
Jianqing Zhu{1}, Shengcai Liao{2}, Stan Z. Li{2}
{1}Huaqiao University, China; {2}Institute of Automation, Chinese Academy of Sciences , China

8:54 ***On Evaluating Perceptual Quality of Online User-Generated Videos***
Soobeom Jang, Jong-Seok Lee
Yonsei University, Korea, South

Internet of Video Things: Enabling Technologies
Time: Monday, May 29 (8:00-9:30)
Room: Grand Ballroom VIII
Chair(s): Eduard Alarcon - Universitat Politècnica de Catalunya; Yen-Kuang Chen - Intel Corporation

8:00 ***INVITED: 3D Machine Vision in IoT for Factory and Building Automation***
Wai Lee
Texas Instruments Inc., United States

8:18 ***A 0.42V High Bandwidth Synthesizable Parallel Access Smart Memory Fabric for Computer Vision***
Prashant Dubey, Kritika Aditya, Ankur Srivastava, Amit Khanuja, Jamil Kawa, Thu Nguyen
SYNOPSYS India Pvt. Ltd., India; SYNOPSYS India Pvt. Ltd., United States

8:36 ***A Color Frame Reproduction Technique for IoT-Based Video Surveillance Application***
Rashedul Hasan, Shahed K. Mohammed, Alimul Haque Khan, Khan A. Wahid
University of Saskatchewan, Canada

8:54 ***Object-Based on-Line Video Summarization for Internet of Video Things***
Shih-Ting Lin{2}, Yuan-Hsin Liao{2}, Yu Tsao{1}, Shao-Yi Chien{2}
{1}Academia Sinica, Taiwan; {2}National Taiwan University, Taiwan

9:12 ***A 142MOPS/mW Integrated Programmable Array Accelerator for Smart Visual Processing***
Satyajit Das{1}, Davide Rossi{1}, Kevin Martin{2}, Philippe Coussy{2}, Luca Benini{1}
{1}Università di Bologna, Italy; {2}Université Bretagne Sud, France

Biometrics & Biomedical Signal/Image Processing Circuits & Systems: I
Time: Monday, May 29 (8:00-9:30)
Room: Grand Ballroom IX
Chair(s): Zhiping Lin - Nanyang Technological University; Danilo Demarchi - Politecnico di Torino

8:00 ***Architecture for Complex Network Measures of Brain Connectivity***
Chandrajit Pal{4}, Dwaipayan Biswas{1}, Koushik Maharatna{3}, Amlan Chakrabarti{2}
{1}IMEC, Belgium; {2}University of Calcutta, India; {3}University of Southampton, United Kingdom; {4}University of Southampton / University of Calcutta, United Kingdom

8:18 ***Non-Invasive Blood Pressure Estimation Using Phonocardiogram***
Amirhossein Esmaili Dastjerdi, Mohammad Kachuee, Mahdi Shabany
Sharif University of Technology, Iran

8:36 ***Towards an on-Chip Signal Processing Solution for the Online Calibration of SS-OCT Systems***
Oscar Barajas, Amir Tofighi Zavareh, Sebastian Hoyos
Texas A&M University, United States

8:54 ***Automatic Endosomal Structure Detection and Localization in Fluorescence Microscopic Images***
Dongyun Lin{1}, Zhiping Lin{1}, Ramraj Velmurugan{2}, Raimund Ober{2}
{1}Nanyang Technological University, Singapore; {2}Texas A&M University, United States

9:12 ***LLC Encoded Bow Features and Softmax Regression for Microscopic Image Classification***
Dongyun Lin{3}, Zhiping Lin{3}, Lei Sun{1}, Kar-Ann Toh{4}, Jiuwen Cao{2}
{1}Beijing Institute of Technology, China; {2}Hangzhou Dianzi University, China; {3}Nanyang Technological University, Singapore; {4}Yonsei University, Korea, South

ADC Circuit Techniques
Time: Monday, May 29 (8:00-9:30)
Room: Grand Ballroom X
Chair(s): Jose Silva-Martinez - Texas A&M University; George Yuan - Hong Kong University of Science and Technology

8:00 ***A 200MS/s, 11 Bit SAR-Assisted Pipeline ADC with Bias-Enhanced Ring Amplifier***
Yongzhen Chen, Jingjing Wang, Hang Hu, Fan Ye, Junyan Ren
Fudan University, China

8:18 ***A 10-b Statistical ADC Employing Pipelining and Sub-Ranging in 32nm CMOS***
Sen Tao{1}, Naveen Verma{1}, Ryan M. Corey{2}, Andrew C. Singer{2}
{1}Princeton University, United States; {2}University of Illinois at Urbana-Champaign, United States

8:36 ***Analog Bandwidth Mismatch Compensation for Time-Interleaved***
Alexandre Mas{2}, Eric Andre{2}, Caroline Lelandais-Perrault{1}, Filipe Vinci Dos Santos{1}, Philippe Benabes{1}
{1}CentraleSupélec, France; {2}STMicroelectronics, France

8:54 ***Sampling Time Calibration Method for Multi-Channel Interleaved ADCs***
Adrian Leuciuc
Cadence Design Systems, United States

9:12 ***A Power Minimized 74 fJ/Conversion-Step 88.6 dB SNR Incremental ΣΔ ADC with an Asynchronous SAR Quantizer***
Saqib Mohamad{2}, Wu Chao{2}, Jie Yuan{2}, Amine Bermak{1}
{1}Hamad Bin Khalifa University / Hong Kong University of Science and Technology, Qatar; {2}Hong Kong University of Science and Technology, Hong Kong

Wireless Communication Receivers for 5G
Time: Monday, May 29 (8:00-9:30)
Room: Laurel AB
Chair(s): Christoph Studer - Rice University; Miroslav Velev - Aries Design Automation

8:00 ***A Wideband Blocker-Resilient Direct ΔΣ Receiver with Selective Input-Impedance Matching***
Faizan Ul Haq{1}, Mikko Englund{1}, Kari Stadius{1}, Marko Kosunen{1}, Jussi Ryynänen{1}, Kimmo Koli{2}, Kim B Östman{3}
{1}Aalto University, Finland; {2}Huawei Technologies Oy Co. Ltd, Finland; {3}Nordic Semiconductor, Finland

8:18 ***An 1.1 V 0.1-1.6 GHz Tunable-Bandwidth Elliptic Filter with 6 dB Linearity Improvement by Precise Zero Location Control in 40 nm CMOS Technology for 5G Applications***
Ching-Da Wu{2}, Jian-Yu Hsieh{1}, Chun-Han Wu{2}, Yang-Sheng Cheng{2}, Chun-Chang Wu{2}, Shey-Shi Lu{2}
{1}National Ilan University, Taiwan; {2}National Taiwan University, Taiwan

8:36 ***Near-Field Dual-Use Antenna for Magnetic-Field Based Communication and Electrical-Field Based Distance Sensing in mm³-Class Sensor Node***
Ryo Shirai{2}, Jin Kono{2}, Tetsuya Hirose{1}, Masanori Hashimoto{2}
{1}Kobe University, Japan; {2}Osaka University, Japan

8:54 ***FPGA Design of Low-Complexity Joint Channel Estimation and Data Detection for Large SIMO Wireless Systems***
Oscar Castañeda{1}, Tom Goldstein{2}, Christoph Studer{1}
{1}Cornell University, United States; {2}University of Maryland, College Park, United States

9:12 ***A Low-Noise Cartesian Error Feedback Architecture***
Jinbo Li, Qun Jane Gu
University of California, Davis, United States

Many-Core Systems
Time: Monday, May 29 (8:00-9:30)
Room: Laurel CD
Chair(s): Vasily Moshnyaga - Fukuoka University; Danella Zhao - University of Louisiana at Lafayette

8:00 ***Dark Silicon-Power-Thermal Aware Runtime Mapping and Configuration in Heterogeneous Many-Core NoC***
Md Farhadur Reza{2}, Dan Zhao{1}, Magdy Bayoumi{2}
{1}Old Dominion University, United States; {2}University of Louisiana at Lafayette, United States

8:18 ***Application Resource Management for Exploitation of Non-Volatile Memory in Many-Core Systems***
Setareh Behroozi, Iraklis Anagnostopoulos
Southern Illinois University Carbondale, United States

8:36 ***Activation of Secure Zones in Many-Core Systems with Dynamic Rerouting***
Luciano Caimi, Vinicius Fochi, Eduardo Wachter, Daniel Munhoz, Fernando Moraes
Pontifícia Universidade Católica do Rio Grande do Sul, Brazil

8:54 ***Demystifying the Cost of Task Migration in Distributed Memory Many-Core Systems***
Marcelo Ruaro, Fernando Moraes
Pontifícia Universidade Católica do Rio Grande do Sul, Brazil

9:12 ***A Low Latency Feature Extraction Accelerator with Reduced Internal Memory***
Rongdi Sun, Peilin Liu, Jun Wang, Zunquan Zhou
Shanghai Jiao Tong University, China

Advanced Video Coding & Standardization
Time: Monday, May 29 (8:00-9:30)
Room: Kent AB
Chair(s): Wen-Hsiao Peng - National Chiao Tung University; Tokunbo Ogunfunmi - Santa Clara University

8:00 ***A Cam Enabled Fast Video Motion Estimation Based on Locality Sensitive Signatures***
Pavel Arnaudov, Dr. Tokunbo Ogunfunmi
Santa Clara University, United States

8:18 ***Fast Intra Coding Unit Size Decision for HEVC with GPU Based Keypoint Detection***
Falei Luo{3}, Shanshe Wang{4}, Siwei Ma{4}, Nan Zhang{2}, Yun Zhou{1}, Wen Gao{4}
{1}Academy of Broadcasting Science, China; {2}Captital Medical University, China; {3}Institute of Computing Technology, Chinese Academy of Sciences, China; {4}Peking University, China

8:36 ***Depth-Projected Determination for Adaptive Search Range in Motion Estimation for HEVC***
Tsz-Kwan Lee, Yui-Lam Chan, Wan-Chi Siu
Hong Kong Polytechnic University, Hong Kong

8:54 ***Measurement-Domain Intra Prediction Framework for Compressively Sensed Images***
Jianbin Zhou, Dajiang Zhou, Li Guo, Yoshimura Takeshi, Satoshi Goto
Waseda University, Japan

9:12 ***A Low-Cost Approximate 32-Point Transform Architecture***
Heming Sun{3}, Zhengxue Cheng{1}, Amir Masoud Gharehbaghi{2}, Shinji Kimura{3}, Masahiro Fujita{2}
{1}Shanghai Jiao Tong University, China; {2}University of Tokyo, Japan; {3}Waseda University, Japan

Mini-Tutorial
Time: Monday, May 29 (8:00-9:30)
Room: Essex AB

8:00 ***Memristor-CMOS hybrid circuits and systems for brain-inspired computing***
Kyeong-Sik Min{1}, Fernando Corinto{2}
Kookmin Univ., Seoul, Korea{1}; Politecnico di Torino, Turin, Italy{2}

Welcome Session and Keynote
Time: Monday, May 29 (9:30-11:00)
Room: Grand Ballroom V-VI

9:30 ***Opening Remarks and Welcome from the Conference Co-Chairs***
Pamela Abshire, University of Maryland, College Park, MD, USA
Ralph Etienne-Cummings, Johns Hopkins University, Baltimore, MD, USA

10:00 ***The BRAIN Initiative: Building, Strengthening, and Sustaining***
Miyoung Chun, Executive VP of Science Programs, The Kavli Foundation

Wearable Sensing Systems
Time: Monday, May 29 (11:30-13:00)
Room: Dover A
Chair(s): Ravinder Dahiya - University of Glasgow; Hadi Heidari - University of Glasgow

11:30 ***Electronic Skin and Electrocutaneous Stimulation to Restore the Sense of Touch in Hand Prosthetics***
Lucia Seminara{3}, Marta Franceschi{3}, Luigi Pinna{3}, Ali Ibrahim{3}, Maurizio Valle{3}, Strahinja Dosen{1}, Dario Farina{2}
{1}Georg-August-Universität Göttingen, Germany; {2}Imperial College London, United Kingdom; {3}Università di Genova, Italy

11:48 ***High Resolution and Linearity Enhanced SAR ADC for Wearable Sensing Systems***
Hua Fan{3}, Hadi Heidari{4}, Franco Maloberti{2}, Dagang Li{1}, Daqian Hu{1}, Yuanjun Cen{1}
{1}Chengdu Sino Microelectronics Technology Co.,Ltd, China; {2}Università degli Studi di Pavia, Italy; {3}University of Electronic Science and Technology of China, China; {4}University of Glasgow, United Kingdom

12:06 ***A Low-Power Low-Noise CMOS Voltage Reference with Improved PSR for Wearable Sensor Systems***
Pınar Başak Başyurt{2}, Edoardo Bonizzoni{3}, Franco Maloberti{3}, Devrim Yilmaz Aksin{1}
{1}Analog Devices Inc., Turkey; {2}Istanbul Technical University, Turkey; {3}Università degli Studi di Pavia, Italy

12:24 ***Information-Processing-Driven Interfaces in Hybrid Large-Area Electronics Systems***
Tiffany Moy, Warren Rieutort-Louis, Liechao Huang, Sigurd Wagner, James Sturm, Naveen Verma
Princeton University, United States

12:42 ***A 310 nW 14.2-Bit Iterative-Incremental ADC for Wearable Sensing Systems***
Tan-Tan Zhang{2}, Man-Kay Law{2}, Bo Wang{1}, Pui-In Mak{2}, Mang-I Vai{2}, Rui Paulo Martins{2}
{1}Hamad Bin Khalifa University / Hong Kong University of Science and Technology, Qatar; {2}University of Macau, Macau

50 years of Circuits, Systems & Signals: A Session in Honor of Prof. Sanjit K. Mitra (Part I)
Time: Monday, May 29 (11:30-13:00)
Room: Dover BC
Chair(s): PP Vaidyanathan - California Institute of Technology; Yao Wang - New York University

11:30 ***A Historical Overview of Dr. Sanjit Mitra's Academic, Research and Professional Activities***
William Jenkins{1}, Michael Soderstrand{2}
{1}Pennsylvania State University, United States; {2}University of California, Davis, United States

11:48 ***Filtering and Enhancement of Color Images in the Block DCT Domain***
Jayanta Mukhopadhyay
Indian Institute of Technology Kharagpur, India

12:06 ***On Secure Communications Without Eavesdropper Channel State***
Phillip Regalia
National Science Foundation / Catholic University of America, United States

12:24 ***INVITED: Photonic Allpass Filter: a Versatile Building Block for All-Optical Signal Processing***
Yujia Wang, Truong Nguyen
University of California, San Diego, United States

Deep Learning Systems
Time: Monday, May 29 (11:30-13:00)
Room: Grand Ballroom I
Chair(s): Jinhu Lu - Chinese Academy of Sciences; Wei Xing Zheng - Western Sydney University

11:30 ***INVITED: Unsupervised Learning Using Adversarial Networks***
Soumith Chintala
Facebook, United States

11:48 ***Pipelined Parallel Contrastive Divergence for Continuous Generative Model Learning***
Bruno Umbria Pedroni, Sadique Sheik, Gert Cauwenberghs
University of California, San Diego, United States

12:06 ***DFGNet: Mapping Dataflow Graph Onto CGRA by a Deep Learning Approach***
Shouyi Yin, Dajiang Liu, Lifeng Sun, Leibo Liu, Shaojun Wei
Tsinghua University, China

12:24 ***Optimizing Deep Neural Network Structure for Face Recognition***
Fanruo Meng, Chang Shu, Hongsheng Liu
University of Electronic Science and Technology of China, China

12:42 ***Evaluation of Neural Network Architectures for Embedded Systems***
Alfredo Canziani{1}, Eugenio Culurciello{1}, Adam Paszke{2}
{1}Purdue University, United States; {2}University of Warsaw, Poland

Brain Circuits & Systems
Time: Monday, May 29 (11:30-13:00)
Room: Grand Ballroom II
Chair(s): Wouter Serdijn - Delft University of Technology; Andreas Demosthenous - University College London

11:30 ***High Density, High Radiance µLED Matrix for Optogenetic Retinal Prostheses and Planar Neural Stimulation***
Ahmed Soltan{3}, Brian McGovern{1}, Emmanuel Drakakis{1}, Mark Neil{1}, Mahbub Akhter{2}, Jun Su Lee{2}, Patrick Degenaar{3}
{1}Imperial College London, United Kingdom; {2}Tyndall National Institute, Ireland; {3}University of Newcastle, United Kingdom

11:48 ***A Precision Pseudo Resistor Bias Scheme for the Design of Very Large Time Constant Filters***
Roberto Puddu, Caterina Carboni, Lorenzo Bisoni, Gianluca Barabino, Danilo Pani, Luigi Raffo, Massimo Barbaro
Università degli Studi di Cagliari, Italy

12:06 ***A High Input Impedance Low Noise Integrated Front-End Amplifier for Neural Monitoring***
Zhijun Zhou, Paul Warr
University of Bristol, United Kingdom

12:24 ***An Integrated Passive Phase-Shift Keying Modulator for Biomedical Implants with Power Telemetry Over a Single Inductive Link***
Dai Jiang, Dominik Cirmirakis, Matthew Schormans, Andreas Demosthenous, Timothy Perkins, Nick Donaldson
University College London, United Kingdom

12:42 ***Memristive Model for Synaptic Circuits***
Yang Zhang{1}, Xiaoping Wang{1}, Yi Li{1}, Eby G. Friedman{2}
{1}Huazhong University of Science and Technology, China; {2}University of Rochester, United States

Oscillators, Phase-locked Loops & Others I
Time: Monday, May 29 (11:30-13:00)
Room: Grand Ballroom III
Chair(s): Jorge Fernandes - Instituto de Engenharia de Sistemas e Computadores-ID; Shahriar Mirabbasi - University of British Columbia

11:30 ***INVITED: a ±10ppm -40 to 125°C BAW-Based Frequency Reference System for Crystal-Less Wireless Sensor Nodes***
Danielle Griffith, Per Torstein Røine, Torjus Kallerud, Brian Goodlin, Zachary Hughes, Ernest Yen
Texas Instruments Inc., Norway; Texas Instruments Inc., United States

11:48 ***On the Mechanisms Governing Spurious Tone Injection in Fractional PLLs***
Federico Bizzarri{1}, Angelo Brambilla{1}, Sergio Callegari{2}
{1}Politecnico di Milano, Italy; {2}Università di Bologna, Italy

12:06 ***A Wide Tuning-Range ADFLL for mW-Socs with Dithering-Enhanced Accuracy in 65 nm CMOS***
David Bellasi, Philipp Schönle, Qiuting Huang, Luca Benini
Eidgenössische Technische Hochschule Zürich, Switzerland

12:24 ***A Novel Segmentation Scheme for DTC-Based ΔΣ Fractional-N PLL***
Tuan Minh Vo, Carlo Samori, Andrea Leonardo Lacaita, Salvatore Levantino
Politecnico di Milano, Italy

12:42 ***0.5 kHz – 32 MHz Digital Fractional-N Frequency Synthesizer with Burst-Frequency Switch***
Seung-Hun Shin, Pil-Ho Lee, Jin-Woo Park, Yu-Jeong Hwang, Young-Chan Jang
Kumoh National Institute of Technology, Korea, South

Temperature Compensated Circuits
Time: Monday, May 29 (11:30-13:00)
Room: Grand Ballroom IV
Chair(s): Degang Chen - Iowa State University; Shahriar Mirabbasi - University of British Columbia

11:30 ***A 0.9V-VDD Sub-nW Resistor-Less Duty-Cycled CMOS Voltage Reference in 65nm for IoT***
Maoqiang Liu, Arthur H. M. van Roermund, Pieter Harpe
Eindhoven University of Technology, Netherlands

11:48 ***A 2.1-ppm/°C Current-Mode CMOS Bandgap Reference with Piecewise Curvature Compensation***
Ruocheng Wang, Wengao Lu, Yuze Niu, Zhaokai Liu, Meng Zhao, Yacong Zhang, Zhongjian Chen
Peking University, China

12:06 ***A Sub-1 V, Nanopower, ZTC Based Zero-VT Temperature-Compensated Current Reference***
David Cordova{1}, Arthur C. de Oliveira{2}, Pedro Toledo{2}, Hamilton Klimach{2}, Sergio Bampi{2}, Eric Fabris{2}
{1}IMS Bordeaux, Peru; {2}Universidade Federal do Rio Grande do Sul, Brazil

12:24 ***Temperature Compensation of Floating-Gate Transistors in Field-Programmable Analog Arrays***
Alexander Dilello{2}, Steven Andryzcik{2}, Brandon Kelly{2}, Brandon Rumberg{1}, David Graham{2}
{1}Aspinity Inc., United States; {2}West Virginia University, United States

12:42 ***A 9-nW on-Chip Constant Subthreshold CMOS Transconductance Bias with Fine-Tuning***
Uldric Antao, John Choma, Theodore Berger
University of Southern California, United States

Computational Image Sensors
Time: Monday, May 29 (11:30-13:00)
Room: Grand Ballroom VII
Chair(s): Joseph Lin - Massachusetts Institute of Technology; Charbel Rizk - Johns Hopkins University

11:30 ***Reducing Electrical Power Dissipation in Computational Imaging Systems Through Special-Purpose Optics***
David Stork, Thomas Vogelsang, James Tringali, Patrick R. Gill, Mark Kellam, Evan Erickson
Rambus Inc., United States

11:48 ***Neuromorphic Readout Integrated Circuits and Related Spike-Based Image Processing***
Dean Scribner, Thomas Petty, Peter Mui
Northrop Grumman Corporation, United States

12:06 ***Characterization of RTN Noise in the Analog Front-End of Digital Pixel Imagers***
Charbel Rizk{2}, Francisco Tejada{1}, John Hughes{2}, David Barbehenn{2}, Philippe Pouliquen{2}, Andreas G. Andreou{2}
{1}Imogin LLC, United States; {2}Johns Hopkins University, United States

12:24 ***Block-Matching Optical Flow for Dynamic Vision Sensors: Algorithm and FPGA Implementation***
Min Liu, Tobi Delbruck
Universität Zürich / Eidgenössische Technische Hochschule Zürich, Switzerland

12:42 ***Spatiotemporal Compressed Sampling for Video Compression***
Jie Zhang, Tao Xiong, Sang Peter Chin, Trac Tran, Ralph Etienne-Cummings
Johns Hopkins University, United States

Internet of Video Things: System Architecture, Framework, & ApplicationTime: Monday, May 29 (11:30-13:00)
Room: Grand Ballroom VIII
Chair(s): Yen-Kuang Chen - Intel Corporation; Eduard Alarcon - Universitat Politècnica de Catalunya

11:30 ***INVITED: Improving Driver Safety Using Deep Learning on Embedded Devices***
David Julian
NetraDyne, United States

11:48 ***Internet of Video Things in 2030: a World with Many Cameras***
Anup Mohan{1}, Kent Gauen{1}, Yung-Hsiang Lu{1}, Wei Wayne Li{2}, Xuemin Chen{2}
{1}Purdue University, United States; {2}Texas Southern University, United State

12:06 ***A Framework for Visual Fog Computing***
Shao-Wen Yang{2}, Omesh Tickoo{2}, Yen-Kuang Chen{1}
{1}Intel Corporation, United States; {2}Intel Research Lablets, United States

12:24 ***A Multi-Agent Based System for Run-Time Distributed Resource Management***
Ioannis Galanis, Daniel Olsen, Iraklis Anagnostopoulos
Southern Illinois University Carbondale, United States

12:42 ***Distributed Video Codec with Spatiotemporal Side Information***
Yueh-Ying Lee{3}, Pin-Hung Kuo{3}, Chia-Han Lee{2}, Yen-Kuang Chen{1}, Shao-Yi Chien{3}
{1}Intel Corporation, United States; {2}National Chiao Tung University, Taiwan; {3}National Taiwan University, Taiwan

Biometrics & Biomedical Signal/Image Processing Circuits & Systems: II
Time: Monday, May 29 (11:30-13:00)
Room: Grand Ballroom IX
Chair(s): Gianluca Setti - Università degli Studi di Ferrara; Danilo Demarchi - Politecnico di Torino

11:30 ***LightProbe: a 64-Channel Programmable Ultrasound Transducer Head with an Integrated Front-End and a 26.4 Gb/s Optical Link***
Pascal Alexander Hager{1}, Christoph Risser{2}, Peter-Karl Weber{2}, Luca Benini{1}
{1}Eidgenössische Technische Hochschule Zürich, Switzerland; {2}Fraunhofer Institute for Biomedical Engineering, Germany

11:48 ***A Microstimulator with Parameter Adjustment for Bladder Dysfunction***
Yu-Jin Lin, Shuenn-Yuh Lee
National Cheng Kung University, Taiwan

12:06 ***On the Use of Compressive Sensing (CS) for Brain Dopamine Recording with Fast-Scan Cyclic Voltammetry (FSCV)***
Hossein Zamani{1}, Hamid Bahrami{3}, Paul Garris{2}, Pedram Mohseni{1}
{1}Case Western Reserve University, United States; {2}Illinois State University, United States; {3}University of Akron, United States

12:24 ***Tensor-Based Fusion of EEG and FMRI to Understand Neurological Changes in Schizophrenia***
Evrim Acar{1}, Yuri Levin-Schwartz{2}, Vince D. Calhoun{3}, Tulay Adalı{2}
{1}University of Copenhagen, Denmark; {2}University of Maryland, Baltimore County, United States; {3}University of New Mexico, United States

12:42 ***A Power-Area-Efficient Impedance Sensor Design for 10 × 10 Microelectrode Array Sensing***
Xinyuan Ge, Tsz Ngai Lin, Jie Yuan
Hong Kong University of Science and Technology, Hong Kong

SAR ADCs
Time: Monday, May 29 (11:30-13:00)
Room: Grand Ballroom X
Chair(s): Mohamad Sawan - Polytechnique Montréal; Jose Silva-Martinez - Texas A&M University

11:30 ***High-Resolution SAR ADC with Enhanced Linearity***
Hua Fan{2}, Franco Maloberti{1}
{1}Università degli Studi di Pavia, Italy; {2}University of Electronic Science and Technology of China, China

11:48 ***Seven-Bit 700-MS/s Four-Way Time-Interleaved SAR ADC with Partial Vcm-Based Switching***
Dezhi Xing{2}, Yan Zhu{2}, Chi-Hang Chan{2}, Sai-Weng Sin{2}, Seng-Pan U{2}, Rui Paulo Martins{2}, Fan Ye{1}, Junyan Ren{1}
{1}Fudan University, China; {2}University of Macau, China; {2}University of Macau, Portugal

12:06 ***A 12-Bit 40-MS/s Calibration-Free SAR ADC***
Chung-Wei Hsu, Li-Jen Chang, Chun-Po Huang, Soon-Jyh Chang
National Cheng Kung University, Taiwan

12:24 ***A Calibration-Free 13-Bit 0.9 V Differential SAR-ADC with Hybrid DAC and Dithering***
Quentin Sauvé{1}, Damien Favre{3}, Gabriel Morin-Laporte{3}, Mohammad Taherzadeh-Sani{2}, Nicolas Constantin{1}, Frédéric Nabki{1}
{1}École de Technologie Supérieure, Canada; {2}Ferdowsi University of Mashhad, Iran; {3}Université du Québec à Montréal, Canada

12:42 ***A Low-Complexity Correlation-Based Time Skew Estimation Technique for Time-Interleaved SAR ADCs***
Armia Salib, Barry Cardiff, Mark Flanagan
University College Dublin, Ireland

MIMO Systems
Time: Monday, May 29 (11:30-13:00)
Room: Laurel AB
Chair(s): Christoph Studer - Rice University; Lan-Da Van - National Chiao Tung University

11:30 ***Power-Aware Space-Time-Trellis-Coded MIMO Detector with SNR Estimation and State-Purging***
Kai-Ting Shr, Chieh-Yu Chen, Jin-Wei Jhang, Yuan-Hao Huang
National Tsing Hua University, Taiwan

11:48 ***ADMM-Based Infinity Norm Detection for Large MU-MIMO: Algorithm and VLSI Architecture***
Shahriar Shahabuddin{2}, Markku Juntti{2}, Christoph Studer{1}
{1}Cornell University, United States; {2}University of Oulu, Finland

12:06 ***A Cholesky Decomposition Based Massive MIMO Uplink Detector with Adaptive Interpolation***
Rakesh Gangarajaiah, Hemanth Prabhu, Ove Edfors, Liang Liu
Lund University, Sweden

12:24 ***Design of an SVD Engine for 8×8 MIMO Precoding Systems***
Chun-Hun Wu, Chin-Yi Liu, Pei-Yun Tsai
National Central University, Taiwan

12:42 ***Algorithm and Architecture for Joint Detection and Decoding for MIMO with LDPC Codes***
Shushen Jing{2}, Junmei Yang{2}, Zhongfeng Wang{1}, Xiaohu You{2}, Chuan Zhang{2}
{1}Nanjing University, China; {2}Southeast University, China

Emerging & Reconfigurable Architectures
Time: Monday, May 29 (11:30-13:00)
Room: Laurel CD
Chair(s): Xinmiao Zhang - Case Western University; Keshab K. Parhi - University of Minnesota at Minneapolis

11:30 ***FPGA Implementation and Comparison of AES-GCM and Deoxys Authenticated Encryption Schemes***
Sandhya Koteshwara{2}, Amitabh Das{1}, Keshab K. Parhi{2}
{1}Intel Corporation, United States; {2}University of Minnesota Twin Cities, United States

11:48 ***Robust 7-nm SRAM Design on a Predictive PDK***
Vinay Vashishtha, Manoj Vangala, Parv Sharma, Lawrence Clark
Arizona State University, United States

12:06 ***A Fast FPGA-Based Deep Convolutional Neural Network Using Pseudo Parallel Memories***
Muluken Hailesellasie, Syed Rafay Hasan
Tennessee Technological University, United States

12:24 ***Fast Cycle-Accurate Compile Based Simulator for Reconfigurable Processor***
Narasinga Rao Miniskar{2}, Raj Narayana Gadde{2}, Young-Chul Rams Cho{1}, Sukjin Kim{1}
{1}Samsung Electronics, Korea, South; {2}Samsung R&D Institute India, Bangalore, India; {2}Samsung R&D Institute India, Bangalore , India

12:42 ***Hierarchical Functional Obfuscation of Integrated Circuits Using a Mode-Based Approach***
Sandhya Koteshwara, Chris H. Kim, Keshab K. Parhi
University of Minnesota Twin Cities, United States

Video Coding Implementations
Time: Monday, May 29 (11:30-13:00)
Room: Kent AB
Chair(s): Saeid Nooshabadi - Michigan Technological University; Lu Yu - Zhejiang University

11:30 ***A Dual-Clock VLSI Design of H.265 Sample Adaptive Offset Estimation for 8K Ultra-HD TV Encoding***
Jianbin Zhou, Dajiang Zhou, Shihao Wang, Shuping Zhang, Takeshi Yoshimura, Satoshi Goto
Waseda University, Japan

11:48 ***H.265/HEVC Encoder Optimization with Parallel-Efficient Algorithm and QP-Based Early Termination***
Caoyang Jiang, Saeid Nooshabadi
Michigan Technological University, United States

12:06 ***A Hardware-Friendly Hierarchical HEVC Motion Estimation Algorithm for UHD Applications***
Li Hu, Jiawei Gu, Guanghui He, Weifeng He
Shanghai Jiao Tong University, China

12:24 ***High-Level Synthesized 2-D IDCT/IDST Implementation for HEVC Codecs on FPGA***
Vili Viitamäki, Panu Sjövall, Jarno Vanne, Timo Hämäläinen
Tampere University of Technology, Finland

12:42 ***A Higher Order Transform Domain Filter Exploiting Non-Local Spatial Correlation for Video Coding***
Qing Zhang, Lu Yu
Zhejiang University, China

Novel Memory Technologies
Time: Monday, May 29 (11:30-13:00)
Room: Essex AB
Chair(s): Alyssa Apsel - Cornell University

11:30 ***Highly Configurable Hybrid GC-eDRAM/SRAM Bitcell for Robust Low-Power Operation***
Robert Giterman{1}, Adam Teman{1}, Pascal Meinerzhagen{2}
{1}Bar-Ilan University, Israel; {2}Intel Research Lablets, United States

11:48 ***Maximization of Crossbar Array Memory Using Fundamental Memristor Theory***
Jason Kamran Jr Eshraghian{1}, Kyoung-Rok Cho{1}, Herbert Ho-Ching Iu{4}, Tyrone Fernando{4}, Sung-Mo Kang{3}, Kamran Eshraghian{2}
{1}Chungbuk National University, Korea, South; {2}iDataMap Corporation, Australia; {3}Korea Advanced Institute of Science and Technology, Korea, South; {4}University of Western Australia, Australia

12:06 ***A Time-Division Multiplexing Signaling Scheme for Low-Power Multi-Drop Memory Links***
Gain Kim{1}, Chen Cao{1}, Kiarash Gharibdoust{2}, Yusuf Leblebici{1}
{1}École Polytechnique Fédérale de Lausanne, Switzerland; {2}Kandou Bus, Switzerland

12:24 ***Dynamic Reference Scheme for Variation-Resilient STT-MRAM Sensing***
Kien Trinh Quang{2}, Sergio Ruocco{1}, Massimo Alioto{2}
{1}Agency for Science, Technology and Research, Singapore; {2}National University of Singapore, Singapore

12:42 ***Universal Performance Parameters for Resistive Switching Devices***
Jorge Gomez{2}, Ioannis Vourkas{2}, Angel Abusleme{2}, Marcos Maestro{3}, Rosana Rodríguez Martínez{3}, Javier Martin-Martinez{3}, Montserrat Nafria{3}, Georgios Ch. Sirakoulis{1}, Antonio Rubio{4}
{1}Democritus University of Thrace, Greece; {2}Pontificia Universidad Católica de Chile, Chile; {3}Universitat Autònoma de Barcelona, Spain; {4}Universitat Politècnica de Catalunya, Spain

Testing & Verification
Time: Monday, May 29 (14:00-15:30)
Room: Dover A
Chair(s): Degang Chen - Iowa State University; Igor Filanvosky - University of Alberta

14:00 ***An Ultra Low-Power Capacitively-Coupled Chopper Instrumentation Amplifier for Wheatstone-Bridge Readout Circuits***
Moaaz Ahmed{2}, Farid Boussaid{3}, Amine Bermak{1}
{1}Hamad Bin Khalifa University / Hong Kong University of Science and Technology, Hong Kong; {2}Hong Kong University of Science and Technology, Hong Kong; {3}University of Western Australia, Australia

14:18 ***Multi-Standard Low-Power DDR I/O Circuit Deisgn in 7nm CMOS Process***
Moo Sung Chae, Thomas Wilson, Eric Naviasky
Cadence Design Systems, United States

14:36 ***A Self-Test on Wafer Level for a MEM Gyroscope Readout Based on ΔΣ Modulation***
Sebastian Nessler, Maximilian Marx, Yiannos Manoli
Albert-Ludwigs-Universität Freiburg / IMTEK, Germany

14:54 ***Accurate Spectral Testing of the Signals with Amplitude Drift***
Yuming Zhuang, Degang Chen
Iowa State University, United States

15:12 ***Floating-Gate FPAA Calibration for Analog System Design and Built-in Self Test***
Sihwan Kim, Sahil Shah, Jennifer Hasler
Georgia Institute of Technology, United States

50 years of Circuits, Systems & Signals: A Session in Honor of Prof. Sanjit K. Mitra (Part II)
Time: Monday, May 29 (14:00-15:30)
Room: Dover BC
Chair(s): PP Vaidyanathan - California Institute of Technology; Yao Wang - New York University

14:00 ***INVITED: Tidbits on Tunable Analog Filters and Image Demosaicing***
Henrique S. Malvar
Microsoft Research, USA

14:18 ***Second-Order Analog Filter Sections with Independently Tunable Center Frequency and Bandwidth***
Antonio Petraglia, Mariane Petraglia, Manoel Perez
Universidade Federal do Rio de Janeiro, Brazil

14:36 ***Unsupervised Video Orchestration Based on Aesthetic Features***
Alessandro Neri, Federica Battisti, Federico Colangelo, Marco Carli
Università degli Studi Roma TRE, Italy

14:54 ***Signal Processing and Climate Understanding***
Jacques Szczupak, Leontina Pinto, Gabriel Torres
Engenho, Brazil

15:12 ***Tunable FIR Digital Filters Using FIR Approximation of Spectral Transformation***
Anamitra Makur
Nanyang Technological University, Singapore

Deep Learning for Embedded Real Time Systems
Time: Monday, May 29 (14:00-15:30)
Room: Grand Ballroom I
Chair(s): Tinoosh Mohsenin - University of Maryland; Azalia Mirhoseini - Google Brain

14:00 ***Tightly Integrated Deep Learning and Symbolic Programming on a Single Neuromorphic Chip***
Bryan Dawson{1}, Jamie Infantolino{2}, Manuel Vindiola{2}, John Monaco{2}
{1}Secure Mission Solutions, United States; {2}U.S. Army Research Laboratory, United States

14:18 ***INVITED: Towards Closing the Energy Gap Between Hog and CNN Features for Embedded Vision***
Amr Suleiman{1}, Yu-Hsin Chen{1}, Joel Emer{2}, Vivienne Sze{1}
{1}Massachusetts Institute of Technology, United States; {2}Massachusetts Institute of Technology / Nvidia Corporation, United States

14:36 ***PACENet: Energy Efficient Acceleration for Convolutional Network on Embedded Platform***
Adwaya Kulkarni, Tahmid Abtahi, Colin Shea, Amey Kulkarni, Tinoosh Mohsenin
University of Maryland, Baltimore County, United States

14:54 ***TinyDL: Just-in-Time Deep Learning Solution for Constrained Embedded Systems***
Bita Darvish Rouhani{2}, Azalia Mirhoseini{1}, Farinaz Koushanfar{2}
{1}Rice University, United States; {2}University of California, San Diego, United States

15:12 ***End-to-End Scalable FPGA Accelerator for Deep Residual Networks***
Yufei Ma, Minkyu Kim, Yu Cao, Sarma Vrudhula, Jae-Sun Seo
Arizona State University, United States

Ultra-efficient Approaches Enabling Long-term, Mobile EEG for Brain Monitoring
Time: Monday, May 29 (14:00-15:30)
Room: Grand Ballroom II
Chair(s): David Hairston - US Army Research Laboratory; Tinoosh Mohsenin - University of Maryland

14:00 ***Wireless Brain Computer Interfaces Enabling Synchronized Optogenetics and Electrophysiology***
Gabriel Gagnon-Turcotte, Léonard L. Gagnon, Guillaume Bilodeau, Benoit Gosselin
Université Laval, Canada

14:18 ***An EEG Artifact Identification Embedded System Using ICA and Multi-Instance Learning***
Ali Jafari{2}, Sunil Gandhi{2}, Harsha Konuru{2}, William David Hairston{1}, Tim Oates{2}, Tinoosh Mohsenin{2}
{1}U.S. Army Research Laboratory, United States; {2}University of Maryland, Baltimore County, United States

14:36 ***Online Adaptive Data Acquisition Enabling Ultra-Low Power Real-World EEG***
Michael Nonte{1}, Joseph Conroy{2}, Peter Gadfort{2}, William David Hairston{2}
{1}DCS Corporation, United States; {2}U.S. Army Research Laboratory, United States

14:54 ***INVITED: Towards Signal Processing Assisted Hardware for Continuous in-Band Electrode Impedance Monitoring***
Siddharth Kohli, Alexander Casson
University of Manchester, United Kingdom

15:12 ***INVITED: Work Towards a Fieldable Multi-Channel EEG System for Continuous Monitoring***
Paul Theilmann{1}, Julian Warchall{2}, Patrick Mercier{2}, Harinath Garudadri{2}
{1}Maxentric Technologies LLC, United States; {2}University of California, San Diego, United States

Oscillators, Phase-locked Loops & Others III
Time: Monday, May 29 (14:00-15:30)
Room: Grand Ballroom III
Chair(s): Nathan Neihart - Iowa State University; Ayman Fayed - Ohio State University

14:00 ***Charge-Controlled Oscillators and Their Application in Frequency Synthesis***
Roohie Kaushik, Shouri Chatterjee, G. S. Visweswaran
Indian Institute of Technology Delhi, India

14:18 ***An Area-Efficient, 0.022-mm², Fully Integrated Resistor-Less Relaxation Oscillator for Ultra-Low Power Real-Time Clock Applications***
Hiroki Asano, Tetsuya Hirose, Toshihiro Ozaki, Nobutaka Kuroki, Masahiro Numa
Kobe University, Japan

14:36 ***A 5-Bit Phase-Interpolator-Based Fractional-N Frequency Divider for Digital Phase-Locked Loops***
Jianfu Lin, Hanjun Jiang, Baoyong Chi
Tsinghua University, China

14:54 ***Below-Ground Injection of Floating-Gate Transistors for Programmable Analog Circuits***
Mir Mohammad Navidi{2}, David Graham{2}, Brandon Rumberg{1}
{1}Aspinity Inc., United States; {2}West Virginia University, United States

15:12 ***Analytic Modeling of Static Noise Margin Considering DIBL and Body Bias Effects***
Fabián Olivera, Antonio Petraglia
Universidade Federal do Rio de Janeiro, Brazil

Innovations in Acoustics
Time: Monday, May 29 (14:00-15:30)
Room: Grand Ballroom IV
Chair(s): Muyinatu Bell - Johns Hopkins University; Ralph Etienne-Cummings - Johns Hopkins University

14:00 ***INVITED: Programmable Electronic Stethoscope***
James E. West, Ian McLane, Mounya Elhilali, Dimitra Emmanouilidou
Johns Hopkins University, United States

14:18 ***Echo Flow Patterns Influence Bat Flight Behavior***
Michaela Warnecke{1}, Benjamin Falk{1}, John Hallam{2}, Cynthia F. Moss{1}
{1}Johns Hopkins University, United States; {2}University of Southern Denmark, United States

14:36 ***INVITED: Automatic Vascular Flow Reconstruction with Doppler Ultrasound***
Xin Kang{2}, David Narrow{2}, Devin O'Brien Coon{1}
{1}Johns Hopkins University, United States; {2}Sonavex, Inc., United States

14:54 ***INVITED: Perceptual Signal Processing for Audio-Visual Beamforming with the Eigenmike Microphone Array and an Omni-Camera***
Daniel R. Mendat, James E. West, Sudarshan Ramenahalli, Ernst Niebur, Andreas G. Andreou
Johns Hopkins University, United States

15:12 ***Advanced Beamforming Methods for Ultrasound and Photoacoustic Imaging***
Muyinatu A. Lediju Bell
Johns Hopkins University, United States

Image Sensors
Time: Monday, May 29 (14:00-15:30)
Room: Grand Ballroom VII
Chair(s): Shoushun Chen - Nanyang Technological University; Viktor Gruev - University of Illinois Urbana-Champaign

14:00 ***A 1600 by 1200, 300 mW, 40 fps Multi-Spectral Imager for Near-Infrared Fluorescence Image-Guided Surgery***
Missael Garcia{2}, Mohamed Zayed{2}, Kyoung-Mi Park{2}, Viktor Gruev{1}
{1}University of Illinois at Urbana-Champaign, United States; {2}Washington University in St. Louis, United States

14:18 ***A Novel Smoothness-Based Interpolation Algorithm for Division of Focal Plane Polarimeters***
Jieyun Zhang{3}, Wenbin Ye{3}, Ashfaq Ahmed{2}, Zhurui Qiu{1}, Yuan Cao{3}, Xiaojin Zhao{3}
{1}Chenghan International School, China; {2}Hong Kong University of Science and Technology, Hong Kong; {3}Shenzhen University, China

14:36 ***Analysis of CMS Noise Reduction for 65 nm CIS***
Raffaele Capoccia, Assim Boukhayma, Christian Enz
École Polytechnique Fédérale de Lausanne, Switzerland

14:54 ***Dead Time Effects in the Indirect Time-of-Fight Measurement with SPADs***
Maik Beer{1}, Olaf Schrey{1}, Bedrich Hosticka{1}, Rainer Kokozinski{2}
{1}Fraunhofer Institute for Microelectronic Circuits and Systems, Germany; {2}Universität Duisburg-Essen, Germany

Energy-Efficient & Secure IoT
Time: Monday, May 29 (14:00-15:30)
Room: Grand Ballroom VIII
Chair(s): Emre Salman - Stony Brook University; Milutin Stanecevic - Stony Brook University

14:00 ***INVITED: Internet of Things and EDA: an Industrial Perspective***
Tuna Tarim
Texas Instruments Inc., United States

14:18 ***Energy Efficient AC Computing Methodology for Wirelessly Powered IoT Devices***
Tutu Wan, Yasha Karimi, Milutin Stanaćević, Emre Salman
Stony Brook University, United States

14:36 ***Variance-Based Digital Logic for Energy Harvesting Internet-of-Things***
Sri Harsha Kondapalli, Xuan Zhang, Shantanu Chakrabartty
Washington Univeristy in St. Louis, USA

14:54 ***A Novel Approximate Computing Based Security Primitive for the Internet of Things***
Mingze Gao, Gang Qu
University of Maryland, College Park, United States

15:12 ***Power Efficient AES Core for IoT Constrained Devices Implemented in 130nm CMOS***
Shady Agwa{1}, Eslam Yahya{3}, Yehea Ismail{2}
{1}American University in Cairo, Egypt; {2}American University in Cairo / Zewail City of Science and Technology, Egypt; {3}American University in Cairo / Zewail City of Science and Technology / Banha University, Egypt

Wireless & Implantable/Injectable Technology Circuits & Systems I
Time: Monday, May 29 (14:00-15:30)
Room: Grand Ballroom IX
Chair(s): Andrew Mason; Virgilio Valente - University College London

14:00 ***A 3-Coil Simultaneous Power and Uplink Data Transmission Inductive Link for Battery-Less Implantable Devices***
Min Li, Dake Liu, Chen Gong, Wan Qiao
Beijing Institute of Technology, Sweden; Beijing Institute of Technology, China

14:18 ***A Rectifier/AC Shunt Regulator Combo Circuit with Inherent AM Demodulation Front-End for Wireless Powered Implants***
Edward Lee
Alfred Mann Foundation, United States

14:36 ***A Wireless Neuroprosthetic for Augmenting Perception Through Modulated Electrical Stimulation of Somatosensory Cortex***
Xilin Liu{2}, Milin Zhang{1}, Xiaotie Wu{1}, Andrew Richardson{2}, Solymar Maldonado{2}, Sam DeLuccia{2}, Yohannes Ghenbot{2}, Timothy Lucas{2}, Jan Van der Spiegel{2}
{1}Tsinghua University, China; {2}University of Pennsylvania, United States

14:54 ***A Wireless System for Combined Heart Optogenetics and Electrocardiography Recording***
Léonard L. Gagnon{2}, Gabriel Gagnon-Turcotte{2}, Aude Popek{2}, Aurélien Chatelier{1}, Mohamed Chahine{2}, Benoit Gosselin{2}
{1}Université de Poitiers, France; {2}Université Laval, Canada

15:12 ***A Model Based Approach for Realizing a Safe Wireless Biotelemetry System***
Kerron Duncan, Ralph Etienne-Cummings
Johns Hopkins University, United States

Sigma-Delta Converters
Time: Monday, May 29 (14:00-15:30)
Room: Grand Ballroom X
Chair(s): George Yuan - Hong Kong University of Science and Technology; Jose Silva-Martinez - Texas A&M University

14:00 ***A Class of 1-Bit Multi-Step Look-Ahead Σ-Δ Modulators***
Charis Basetas, Thanasis Orfanos, Paul Peter Sotiriadis
National Technical University of Athens, Greece

14:18 ***Passive Loop Filter Assistance for CTSDMs***
Dries Vercaemer, Johan Raman, Pieter Rombouts
Ghent University, Belgium

14:36 ***Current-Mode Multi-Path Excess Loop Delay Compensation for GHz Sampling CT ΣΔ ADCs***
Chenming Zhang{1}, Lucien J. Breems{2}, Georgi Radulov{1}, Muhammed Bolatkale{2}, Qilong Liu{1}, Hans Hegt{1}, Arthur H. M. van Roermund{1}
{1}Eindhoven University of Technology, Netherlands; {2}NXP Semiconductors N.V., Netherlands

14:54 ***A 3rd Order MASH Switched-Capacitor ΣΔM Using Ultra Incomplete Settling Employing an Area Reduction Technique***
David Fouto{1}, Nuno Paulino{2}
{1}Universidade Nova de Lisboa, Portugal; {2}Universidade Nova de Lisboa / CTS-UNINOVA, Portugal

15:12 ***Subtractive Dithering Technique for Delta-Sigma Modulator***
Zhichao Tan, Roberto Maurino, Robert Adams, Khiem Nguyen
Analog Devices Inc., Italy; Analog Devices Inc., United States

Communication Circuits and Systems
Time: Monday, May 29 (14:00-15:30)
Room: Laurel AB
Chair(s): Zhiyuan Yan - Lehigh University; Christoph Studer - Rice University

14:00 ***Spurs-Free Single-Bit-Output All-Digital Frequency Synthesizers with Forward and Feedback Spurs and Noise Cancellation***
Paul Peter Sotiriadis
National Technical University of Athens, Greece

14:18 ***An Efficient Parallel Resampling Structure Based on Iterated Short Convolution Algorithm***
Hao Li{1}, Jie Guo{2}, Zhigang Wang{1}, Houjun Wang{1}
{1}University of Electronic Science and Technology of China, China; {2}University of Pittsburgh, United States

14:36 ***A Low-Voltage High-Swing Colpitts VCO with Inherent Tapped Capacitors Based Dynamic Body Bias Technique***
Jun Chen, Benqing Guo, Fading Zhao, Yao Wang, Guangjun Wen
University of Electronic Science and Technology of China, China

14:54 ***Asychnronous Sampling Based Hybrid Equalizer***
Namik Kocaman{1}, Michael Green{2}
{1}Broadcom Ltd., United States; {2}University of California, Irvine, United States

15:12 ***A High Temperature Variable Gain Amplifier Based on GaN HEMT Devices for Downhole Communications***
Mohammed Ehteshamuddin, Jebreel Salem, Dong Ha
Virginia Polytechnic Institute and State University, United States

Low Power Architectures
Time: Monday, May 29 (14:00-15:30)
Room: Laurel CD
Chair(s): Zhiyuan Yan - Lehigh University; Yun Chen - Fudan University

14:00 ***Dark Memory and Accelerator-Rich System Optimization in the Dark Silicon Era***
Ardavan Pedram{2}, Stephen Richardson{2}, Mark Horowitz{2}, Shahar Kvatinsky{3}, Sameh Galal{1}
{1}Citadel LLC, United States; {2}Stanford University, United States; {3}Technion – Israel Institute of Technology, Israel

14:18 ***Integration of Energy-Recycling Logic and Wireless Power Transfer for Ultra-Low-Power Implantables***
Hsin-Tzu Lin{1}, Yi-Chung Wu{2}, Ping-Hsuan Hsieh{3}, Chia-Hsiang Yang{2}
{1}National Chiao Tung University, Taiwan; {2}National Taiwan University, Taiwan; {3}National Tsing Hua University, Taiwan

14:36 ***Seeking Low-Power Synchronous/Asynchronous Systems: a FIR Implementation Case Study***
Ali Skaf{1}, Jean Simatic{2}, Laurent Fesquet{2}
{1}Syrian Private University, Syria; {2}Université Grenoble Alpes / TIMA Laboratory, France

14:54 ***Reducing Power, Area, and Delay of Threshold Logic Gates Considering Non-Integer Weights***
Seyed Nima Mozaffari, Spyros Tragoudas, Themistoklis Haniotakis
Southern Illinois University Carbondale, United States

15:12 ***Power-Rail ESD Clamp Circuit with Hybrid-Detection Enhanced Triggering in a 65-nm, 1.2-V CMOS Process***
Guangyi Lu, Yuan Wang, Yize Wang, Xing Zhang
Peking University, China

Visual Signal Enhancement, Presentation & Analysis
Time: Monday, May 29 (14:00-15:30)
Room: Kent AB
Chair(s): Chris Lee - National Cheng Kung University; Wan-Chi Siu - Hong Kong Polytechnic University

14:00 ***Image Co-Segmentation via Saliency Co-Fusion***
Koteswar Rao Jerripothula{1}, Jianfei Cai{2}, Junsong Yuan{2}
{1}Graphic Era University, India; {2}Nanyang Technological University, Singapore

14:18 ***Complexity Reduction by Modified Scale-Space Construction in Sift Generation Optimized for a Mobile GPU***
Chulhee Lee{2}, Hyuk-Jae Lee{2}, Chae Eun Rhee{1}
{1}Inha University, Korea, South; {2}Seoul National University, Korea, South

14:36 ***Low-Lighting Video Enhancement Using Constrained Spatial-Temporal Model for Real-Time Mobile Communication***
Xinwei Gao, Haibo Deng, Yaoyao Guo, Chenchen Gu, Yongfang Shi, Anlin Gao, Licai Guo, Xunan Mao, Jing Lv
Tencent Holdings Limited, China

14:54 ***Detection of Abandoned Objects Using Robust Subspace Recovery with Intrinsic Video Alignment***
Lucas Thomaz{2}, Allan Da Silva{2}, Eduardo Da Silva{2}, Sergio Netto{2}, Hamid Krim{1}
{1}North Carolina State University, United States; {2}Universidade Federal do Rio de Janeiro, Brazil

15:12 ***Subpixel Rendering Without Color Distortions for Diamond-Shaped PenTile Displays***
Jae-Han Lee, Kyung-Rae Kim, Chang-Su Kim
Korea University, Korea, South

ULP Circuits for Implantables & Wearables
Time: Monday, May 29 (14:00-15:30)
Room: Essex AB
Chair(s): Alyssa Apsel - Cornell University

14:00 ***A Chopper Capacitively-Coupled Instrumentation Amplifier Capable of Handling Large Electrode Offset for Biopotential Recordings***
Jiawei Zheng, Wing-Hung Ki, Langyu Hu, Chi-Ying Tsui
Hong Kong University of Science and Technology, Hong Kong

14:18 ***Self-Sustainable Smart Ring for Long Term Monitoring of Blood Oxygenation***
Petar Jokic, Giovanni Antonio Salvatore, Michele Magno, Lars Büthe, Gerhard Tröster, Luca Benini
Eidgenössische Technische Hochschule Zürich, Switzerland

14:36 ***0.4-to-1-V Voltage Scalable ΔΣ ADC with Two-Step Hybrid Integrator for IoT Sensor Applications in 65nm LP CMOS***
Jun-Eun Park, Young-Ha Hwang, Deog-Kyoon Jeong
Seoul National University, Korea, South

14:54 ***Kinetic AC/DC Converter for Electromagnetic Energy Harvesting in Autonomous Wearable Systems***
Robin Bolt{1}, Michele Magno{1}, Thomas Burger{1}, Aldo Romani{2}, Luca Benini{1}
{1}Eidgenössische Technische Hochschule Zürich, Switzerland; {2}Università di Bologna, Italy

15:12 ***Dual-Band Wireless Power Transfer System Using Circular Defected Ground Structure Resonators for Biomedical Applications***
Fairus Tahar, Adel Barakat, Redzuan Saad, Kuniaki Yoshitomi, Ramesh Pokharel
Kyushu University, Japan

CASS STUDENT DESIGN COMPETITION – MONDAY, MAY 29TH

CASS Student Design Competition
Time: Monday, May 29 (14:00-15:30)
Room: Atlantic
Chair(s): Eduardo da Silva - Universidade Federal do Rio de Janeiro

INDEPENDENT CLEANING ROBOT USING THE OPEN-HARDWARE PLATFORM ARDUINO
Beatriz Pontes Silva, Bryan Leite dos Santos, Eduardo Nascimento Emerich, Gabriella Duarte Silva Silveira, Gabrielle Silva de Andrade, Igor Menezes Santos, Isabella Barbosa Oliveira de Macedo, Izabele Bonfim Barbosa, Jean Paul Robert Barbosa Cerqueira, Viviane Cardoso Alves
Centro Federal de Educação Tecnológica Celso Suckow da Fonseca (CEFET/RJ), Nova Iguaçu, RJ, Brazil

AUTOMATED MINIATURE GREENHOUSE FOR DOMESTIC ORGANIC GARDEN
Beatriz Pontes Silva, Bryan Leite dos Santos, Eduardo Nascimento Emerich, Gabriella Duarte Silva Silveira, Gabrielle Silva de Andrade, Igor Menezes Santos, Isabella Barbosa Oliveira de Macedo, Izabele Bonfim Barborsa, Viviane Cardoso Alves
Centro Federal de Educação Tecnológica Celso Suckow da Fonseca (CEFET/RJ), Nova Iguaçu, RJ, Brazil

A MAN-MACHINE INTERACTION SYSTEM BASED ON EEG, EOG AND MACHINE LEARNING
Yufei Hu{1}, Qirui Zhang{1}, Xiaoyi Sun{1}, Bo Zhang{1}, Min Li{2}, Yufan Zhou{3}
{1}Shanghai Jiao Tong University, Shanghai, China; {2}Shanghai Jiao Tong University, Shanghai, China; {3}Shanghai Jin Shan High School, Shanghai, China

SMART PET CLOTHING: GUARDIAN OF HEALTH AND MOOD
Yu-Jin Lin{1}, Yao-Tse Chang{1}, Hao-Yun Lee{1}, Zhan-Xian Liao{1}, You-Ren Du{1}, Yi-Wu Hung{2}, and Hao-Yu Tsai{2}
{1}National Cheng-Kung University, Tainan, Taiwan; {2} Tainan First High School, Tainan, Taiwan

***CASS Student Design Competition posters/demos will subsequently be on display in the poster hall in Harborside Ballroom during the Tuesday Poster Session from 15:00-16:30.*

LIVE DEMONSTRATIONS – MONDAY, MAY 29TH

Demonstration Session I
Time: Monday, May 29 (14:00-17:00)
Room: Harborside Ballroom
Chair(s): Jennifer Blain Christen - Arizona State University; Shih-Chii Liu - Swiss Federal Institute of Technology in Zurich

O-1 - Live Demonstration: Photon Counting and Direct ToF Camera Prototype Based on CMOS SPADs
Ion Vornicu, Ricardo Carmona-Galán, Ángel Rodríguez-Vázquez
Consejo Superior de Investigaciones Científicas / Universidad de Sevilla, Spain

O-2 - Live Demonstration: a 1600 by 1200, 300 mW, 40 fps Multi-Spectral Imager for Near-Infrared Fluorescence Image-Guided Surgery
Missael Garcia{2}, Mohamed Zayed{2}, Kyoung-Mi Park{2}, Viktor Gruev{1}
{1}University of Illinois at Urbana-Champaign, United States; {2}Washington University in St. Louis, United States

O-3 - Live Demonstration: Event-Driven Real-Time Spoken Digit Recognition System
Jithendra Anumula, Daniel Neil, Xiaoya Li, Tobi Delbruck, Shih-Chii Liu
Universität Zürich / Eidgenössische Technische Hochschule Zürich, Switzerland

O-4 - Live Demonstration: Hardware Implementation of Convolutional STDP for on-Line Visual Feature Learning
Amirreza Yousefzadeh{1}, Timothee Masquelier{2}, Teresa Serrano-Gotarredona{1}, Bernabe Linares-Barranco{1}
{1}Consejo Superior de Investigaciones Científicas / Universidad de Sevilla, Spain; {2}Massachusetts Institute of Technology, France

O-5 - Live Demonstration: Multiplexing AER Asynchronous Channels Over LVDS Links with Flow-Control and Clock-Correction for Scalable Neuromorphic Systems
Amirreza Yousefzadeh{2}, Miroslav Jabłoński{1}, Taras Iakymchuk{4}, Alejandro Linares-Barranco{3}, Alfredo Rosado{4}, Luis Plana{5}, Teresa Serrano-Gotarredona{2}, Steve Furber{5}, Bernabe Linares-Barranco{2}
{1}AGH University of Science and Technology, Poland; {2}Consejo Superior de Investigaciones Científicas / Universidad de Sevilla, Spain; {3}Universidad de Sevilla, Spain; {4}Universitat de València, Spain; {5}University of Manchester, United Kingdom

O-6 - Live Demonstration: Dynamic Voltage and Frequency Scaling for Neuromorphic Many-Core Systems
Sebastian Höppner{1}, Yexin Yan{1}, Bernhard Vogginger{1}, Andreas Dixius{1}, Johannes Partzsch{1}, Prateek Joshi{1}, Felix Neumärker{1}, Stephan Hartmann{1}, Stefan Schiefer{1}, Stefan Scholze{1}, Georg Ellguth{1}, Love Cederstroem{1}, Matthias Eberlein{1}, Christian Mayr {1}, Steve Temple {2}, Luis Plana {2}, Jim Garside{2}, Simon Davison {2},David R. Lester {2}, Steve Furber{2}
{1}Technische Universität Dresden, Germany; {2}University of Manchester, United Kingdom

O-7 - Live Demonstration: a 768×640 Pixels 200Meps Dynamic Vision Sensor
Menghan Guo, Jing Huang, Shoushun Chen
Nanyang Technological University, Singapore

O-8 - Live Demonstration: a TiO2 ReRAM Parameter Extraction Method
Ioannis Messaris{1}, Spyridon Nikolaidis{1}, Alexantrou Serb{2}, Spyros Stathopoulos{2}, Isha Gupta{2}, Ali Khiat{2}, Themistoklis Prodromakis{2}
{1}Aristotle University of Thessaloniki, Greece; {2}University of Southampton, United Kingdom

O-9 - Live Demonstration: mNET: a Visually Rich Memristor Crossbar Simulator
Radu Berdan{1}, Alexantrou Serb{2}, Christos Papavassiliou{1}, Themistoklis Prodromakis{2}
{1}Imperial College London, United Kingdom; {2}University of Southampton, United Kingdom

O-10 - Live Demonstration: a Pulsar Signal Receiver System for Navigation
Diogo Brito, Joao Santos, Jorge Fernandes, Gonçalo Tavares
Universidade Técnica de Lisboa / Instituto de Engenharia de Sistemas e Computadores - Investigação , Portugal

O-11 - Live Demonstration: FPGA Demonstration of Spiking Support Vector Networks Based on Growth Transform Neurons
John Mackay, Ahana Gangopadhyay, Shantanu Chakrabartty
Washington University in St. Louis, United States

O-12 - Live Demonstration: Feature Extraction System Using Restricted Boltzmann Machines on FPGA
Kodai Ueyoshi{2}, Takao Marukame{3}, Tetsuya Asai{2}, Masato Motomura{2}, Alexandre Schmid{1}
{1}École Polytechnique Fédérale de Lausanne, Switzerland; {2}Hokkaido University, Japan; {3}Toshiba Corporation, Japan

O-13 - Live Demonstration: Convolutional Neural Network Driven by Dynamic Vision Sensor Playing RoShamBo
Iulia-Alexandra Lungu, Federico Corradi, Tobi Delbruck
Universität Zürich / Eidgenössische Technische Hochschule Zürich, Switzerland

O-14 - Live Demonstration - Multilayer Spiking Neural Network for Audio Samples Classification Using SpiNNaker
Juan P. Dominguez-Morales, Antonio Rios-Navarro, Daniel Gutierrez-Galan, Ricardo Tapiador-Morales, Angel Jimenez-Fernandez, Elena Cerezuela-Escudero, Manuel J. Dominguez-Morales, Alejandro Linares-Barranco
Universidad de Sevilla, Spain

O-15 - Live Demonstration: a Compact All-CMOS Spatiotemporal Compressed Sensing Video Camera

Tao Xiong{2}, Jie Zhang{3}, Chetan Singh Thakur{2}, John Rattray{2}, Sang Chin{1}, Trac Tran{2}, Ralph Etienne-Cummings{2}
{1}Boston University, United States; {2}Johns Hopkins University, United States; {3}Massachusetts Institute of Technology, United States

O-16 - Live Demonstration: Event-Based Image Processing on CMOS Mihalas-Niebur Neuron Array Transceiver

Jamal Molin, Adebayo Eisape, Ralph Etienne-Cummings
Johns Hopkins University, United States

O-17 - Live Demonstration: FPGA Neural Array Emulation for Real-Time, Event-Based Simultaneous Dewarping and Filtering for Aerial Vehicles

Jamal Molin, John Rattray, Ralph Etienne-Cummings
Johns Hopkins University, United States

O-18 - Live Demonstration: a Stimulation Platform for Optogenetic and Bionic Vision Restoration

Francesco Galluppi{2}, Guillaume Chenegros{3}, Didier Pruneau{2}, Gilles Cordurié{3}, Charlie Galle{3}, Nicolas Oddo{3}, Xavier Lagorce{1}, Christoph Posch{1}, Joel Chavas{2}, Ryad Benosman{3}
{1}Chronocam, France; {2}Gensight Biologics, France; {3}Université Pierre-et-Marie-Curie, France

POSTER SESSION – MONDAY, MAY 29TH

Sensory Systems
Time: Monday, May 29 (15:30-17:00)
Room: Harborside Ballroom
Chair(s): Piotr Dudek - The University of Manchester; Timothy Constandinou - Imperial College London

O-19 - Photon Counting and Direct ToF Camera Prototype Based on CMOS SPADs
Ion Vornicu, Ricardo Carmona-Galán, Ángel Rodríguez-Vázquez
Consejo Superior de Investigaciones Científicas / Universidad de Sevilla, Spain

O-20 - Highly Linear Integrate-and-Fire Modulators with Soft Reset for Low-Power High-Speed Imagers
Michele Dei, Roger Figueras, Josep Maria Margarit, Lluís Terés, Francisco Serra-Graells
Consejo Superior de Investigaciones Científicas, Spain

O-21 - Color Temporal Contrast Sensitivity in Dynamic Vision Sensors
Diederik Paul Moeys{3}, Chenghan Li{3}, Julien N.P. Martel{3}, Simeon Bamford{2}, Luca Longinotti{2}, Vasyl Motsnyi{1}, David San Segundo Bello{1}, Tobi Delbruck{3}
{1}IMEC, Belgium; {2}iniLabs GmbH, Switzerland; {3}Universität Zürich / Eidgenössische Technische Hochschule Zürich, Switzerland

O-22 - Real-Time Trajectory Calculation and Prediction Using Neighborhood-Level Parallel Processing
Mahir Gharzai, Dingyi Hong, Joseph Schmitz, Michael Hoffman, Sina Balkir
University of Nebraska-Lincoln, United States

O-23 - Dark Current Reduction by an Adaptive CTIA Photocircuit for Room Temperature SWIR Sensing
Andrew Berkovich{3}, Alexander Castro{3}, Mohammad Islam{2}, Fow-Sen Choa{2}, Geoffrey Barrows{1}, Pamela Abshire{3}
{1}Centeye, Inc., United States; {2}University of Maryland, Baltimore County, United States; {3}University of Maryland, College Park, United States

O-24 - A Battery-Less, 255 Na Quiescent Current Temperature Sensor with Voltage Regulator Fully Powered by Harvesting Ambient Vibrational Energy
Shiquan Fan, Liuming Zhao, Peng Wang, Ran Wei, Xu-Qian Zheng, Zenghui Wang, Philip X.-L. Feng
Case Western Reserve University, United States

O-25 - A Passively Compensated Capacitive Sensor Readout with Biased Varactor Temperature Compensation and Temperature Coherent Quantization
Yong Wang{2}, Yan Hong{2}, Wang Ling Goh{2}, Kevin Chai{1}, Xin Lou{3}, Wenbin Ye{4}
{1}Agency for Science, Technology and Research / Nanyang Technological University, Singapore; {2}Nanyang Technological University, Singapore; {3}ShanghaiTech University, China; {4}Shenzhen University, China

O-26 - Optimum Synchronous Phase Detection and its Application in Smart Sensor Interfaces
Sining Pan, Kofi Makinwa
Technische Universiteit Delft, Netherlands

Biomedical Signal Processing
Time: Monday, May 29 (15:00-17:30)
Room: Harborside Ballroom
Chair(s): Nitish Thakor - Johns Hopkins University; Timothy Constandinou - Imperial College London

P-27 - Motion Artifact Reduction from PPG Signals During Intense Exercise Using Filtered X-LMS
Khawaja Taimoor Tanweer{1}, Syed Rafay Hasan{2}, Awais Mehmood Kamboh{1}
{1}National University of Sciences and Technology, Pakistan; {2}Tennessee Technological University, United States

P-28 - An Accurate Method for Fourier Synthesis of Photoplethysmographic Signals
Saman Abeysekera
Nanyang Technological University, Singapore

P-29 - An Optical Tracker Based Registration Method Using Feedback for Robot-Assisted Insertion Surgeries
Zhuo Li, Xingtong Liu, Xiang Xie, Guolin Li, Songping Mai, Zhihua Wang
Tsinghua University, China

P-30 - Palmprint Recognition Using Deep Scattering Network
Shervin Minaee, Yao Wang
New York University, United States

P-31 - On-Chip ID Generation for Multi-Node Implantable Devices Using SA-PUF
Chang Gao, Sara Ghoreishizadeh, Yan Liu, Timothy Constandinou
Imperial College London, United Kingdom

P-32 - An Aided Information to Characterize ECG Signals as Normal or Abnormal
Krupa Bhavsar, Hen-Geul Yeh, Perla Ayala
California State University, Long Beach, United States

P-33 - An Accurate Automatic System for Distinguishing Neuropathy and Healthy Electromyography Signals
Salim Lahmiri{1}, Mounir Boukadoum{2}
{1}École de Technologie Supérieure, Canada; {2}Université du Québec à Montréal, Canada

P-34 - Real-Time Clustering Algorithm That Adapts to Dynamic Changes in Neural Recordings
Sylmarie Dávila-Montero{2}, Deren Barsakcioglu{1}, Andrew Jackson{3}, Timothy Constandinou{1}, Andrew J. Mason{2}
{1}Imperial College London, United Kingdom; {2}Michigan State University, United States; {3}University of Newcastle, United Kingdom

P-35 - Receiver Echo Cancellation with Real-Time Self Calibration for Passive Implanted Neuron Recorders
Maryam Shafiee, Sule Ozev
Arizona State University, United States

P-36 - 32-Channel Ultra-Low-Noise Arbitrary Signal Generation Platform for Biopotential Emulation
Dorian Haci, Yan Liu, Timothy Constandinou
Imperial College London, United Kingdom

Optimization and Manufacturability
Time: Monday, May 29 (15:30-17:00)
Room: Harborside Ballroom
Chair(s): Meng-Fan Chang - National Tsing Hua University; Gehm Moraes - Pontifical Catholic University of Rio Grande do Sul

Q-37 - Efficient SVM-Based Hotspot Detection Using Spectral Clustering
Fan Yang{1}, Charles C. Chiang{2}, Xuan Zeng{1}, Dian Zhou{1}
{1}Fudan University, China; {2}SYNOPSYS India Pvt. Ltd., United States

Q-38 - Non-Linear Library Characterization Method for FinFET Logic Cells by L1-Minimization
Byung Su Kim{2}, Hyo Sig Won{3}, Tae Hee Han{1}, Joon-Sung Yang{3}
{1}Samsung Electronics, Korea, South; {2}Samsung Electronics / Sungkyunkwan University, Korea, South; {3}Sungkyunkwan University, Korea, South

***Q-39 -* A Grid-Based Detailed Routing Algorithm for Advanced 1D Process**
Ye Zhang{1}, Fan Yang{1}, Dian Zhou{1,3}, Xuan Zeng{1} and Xiangdong Hu{2}
{1}State Key Lab of ASIC & System, School of Microelectronics, Fudan University, China; {2}Shanghai High-Performance Integrated-Circuit Design Center, China; {3}University of Texas at Dallas, USA

Q-40 - Design of a Digital IP for 3D-IC Die-to-Die Clock Synchronization
Mehdi Sadi{2}, Sukeshwar Kannan{1}, Luke England{1}, Mark Tehranipoor{2}
{1}GLOBALFOUNDRIES US Inc., United States; {2}University of Florida, United States

Q-41 - A Survey of Path Search Algorithms for VLSI Detailed Routing
Stèphano Gonçalves, Leomar Da Rosa Jr., Felipe Marques
Universidade Federal de Pelotas, Brazil

Q-42 - Power-Efficient, Gate-Based Digital-to-Time Converter in CMOS
Øystein Bjørndal, Tor Sverre Lande
University of Oslo, Norway

Q-43 - Impacts of Different Shapes of Through-Silicon-Via Core on 3D IC Performance
Abdul Hamid Yousuf, Nahid Hossain, Masud Chowdhury
University of Missouri–Kansas City, United States

Q-44 - Stability of Rotary Traveling Wave Oscillators Under Process Variations and NBTI
Ragh Kuttappa, Leo Filippini, Scott Lerner, Baris Taskin
Drexel University, United States

Q-45 - A Multi-Measurements RO-TDC Implemented in a Xilinx Field Programmable Gate Array
Safa Berrima{2}, Yves Blaquière{1}, Yvon Savaria{2}
{1}École de Technologie Supérieure, Canada; {2}Polytechnique Montréal, Canada

Q-46 - On the Use of Approximate Adders in Carry-Save Multiplier-Accumulators
Darjn Esposito, Davide De Caro, Ettore Napoli, Nicola Petra, Antonio Strollo
Università degli Studi di Napoli Federico II, Italy

Q-47 - A Framework to Automatically Generate Heterogeneous Organization Reconfigurable Multiprocessing
Josimar Sfreddo{1}, Rafael Fão de Moura{1}, Michael Guilherme Jordan{1}, Jeckson Souza{2}, Antonio Carlos Schneider Beck{2}, Mateus Beck Rutzig{1}
{1}Universidade Federal de Santa Maria, Brazil; {2}Universidade Federal do Rio Grande do Sul, Brazil

Q-48 - Efficient Computation of the Sensitization Probability of a Critical Path Considering Process Variations and Path Correlation
Pavan Kumar Javvaji, Spyros Tragoudas
Southern Illinois University Carbondale, United States

Q-49 - A Low Cost Technique for Scan Chain Diagnosis
Satyadev Ahlawat, Darshit Vaghani, Rohini Gulve, Virendra Singh
Indian Institute of Technology Bombay, India

Q-50 - Robustness of Sub-22nm Multigate Devices Against Physical Variability
Alexandra Lackmann Zimpeck{2}, Ygor Aguiar{2}, Cristina Meinhardt{1}, Ricardo Reis{2}
{1}Universidade Federal do Rio Grande, Brazil; {2}Universidade Federal do Rio Grande do Sul, Brazil

Q-51 - METS: a Multiple Event Transient Simulator
Adam Watkins, Spyros Tragoudas
Southern Illinois University Carbondale, United States

Communication Methods
Time: Monday, May 29 (15:30-17:00)
Room: Harborside Ballroom
Chair(s): Hsi-Pin Ma - National Tsing Hua University; Tokunbo Ogunfunmi - Santa Clara University

R-52 - A 8-Gb/s 0.256-pJ/b Transceiver for 5-mm on-Chip Interconnects in 130-nm CMOS
Xiangdong Jia, Glenn Cowan
Concordia University, Canada

R-53 - A 17.5-Gb/s Transceiver with a MaxEye-Based Autonomous Adaptation
Jahoon Jin, Xuefan Jin, Sang-Hoon Kim, Ik-Hwan Kim, Jaehong Jung, Kiwon Kwon, Jung-Hoon Chun
Sungkyunkwan University, Korea, South

R-54 - A 25 Gb/s 470 µW Active Inductor Equalizer for Ground Referenced Signaling Receivers
Laura Fick{2}, Dennis Sylvester{2}, John Poulton{1}, John Wilson{1}, Tom Gray{1}
{1}Nvidia Corporation, United States; {2}University of Michigan, United States

R-55 - Secure Authentication and Access Mechanism for IoT Wireless Sensors
Mahzad Azarmehr, Arash Ahmadi, Rashid Rashidzadeh
University of Windsor, Canada

R-56 - A 170nW CMOS Wake-Up Receiver with -60 dBm Sensitivity Using AlN High-Q Piezoelectric Resonators
Scott Block, Xiaonan Jiang, Brad Harris, Can Cui, Jeronimo Segovia Fernandez, Rajeevan Amirtharajah, Dave Horsley, Hooman Rashtian, Xiaoguang Liu
University of California, Davis, United States

R-57 - High Temperature VCO Based on GaN Devices for Downhole Communications
Tianming Feng, Jebreel Salem, Dong Ha
Virginia Polytechnic Institute and State University, United States

R-58 - A 9.4 pJ/Bit 432 MHz 16-QAM/MSK Transmitter Based on Edge-Combining Power Amplifier
Yanshu Guo, Songping Mai, Zhaoyang Weng, Heng Liu, Hanjun Jiang, Zhihua Wang
Tsinghua University, China

R-59 - Adaptive Baseband Pre-Equalization for RF Impedance Matching Correction
Cyro Hemsi, Cristiano Panazio
Universidade de São Paulo, Brazil

R-60 - On Envelope-Tracking for SOA Amplification of Multicarrier Signals
Julio-Cesar Ortiz Cornejo{2}, Serban Bejan{3}, Stéphane Azou{1}, Jorge-Arturo Pardinas Mir{2}, Pascal Morel{1}
{1}École nationale d'ingénieurs de Brest, France; {2}Instituto Tecnológico y de Estudios Superiores de Occidente, Mexico; {3}Military Technical Academy, Romania

R-61 - A 1 – 8 Gb/s Optical Wireless Communication Dual-Mode Receiver
Waichiu Ng, Jie Yuan
Hong Kong University of Science and Technology, Hong Kong

R-62 - 16-Channel Modular Platform for Automatic Control and Reconfiguration of Complex Photonic Circuits
Emanuele Guglielmi, Marco Carminati, Francesco Zanetto, Andrea Annoni, Francesco Morichetti, Andrea Melloni, Marco Sampietro, Giorgio Ferrari
Politecnico di Milano, Italy

R-63 - Phase Noise Analysis of a Homodyne Radar System Driven by a Phase-Locked Loop
Frank Herzel, Dietmar Kissinger
IHP GmbH, Germany

R-64 - Multi Component Carrier, Sub-Band DPD and GNURadio Implementation
Chance Tarver{1}, Mahmoud Abdelaziz{2}, Lauri Anttila{2}, Joseph Cavallaro{1}
{1}Rice University, United States; {2}Tampere University of Technology, Finland

R-65 - Design Guidelines for the High-Speed Dynamic Partial Reconfiguration Based Software Defined Radio Implementations on Xilinx Zynq FPGA
Ahmed Kamaleldin{2}, Ahmed Mohamed{2}, Ahmed Nagy{2}, Youssef Gamal{2}, Ahmed Shalash{2}, Yehea Ismail{1}, Hassan Mostafa{3}
{1}American University in Cairo / Zewail City of Science and Technology, Egypt; {2}Cairo University, Egypt; {3}Cairo University / American University in Cairo / Zewail City of Science and Technology, Egypt

Video Signal Processing & Coding Algorithms
Time: Monday, May 29 (15:30-17:00)
Room: Harborside Ballroom
Chair(s): Qi Tian - University of Texas at San Antonio; Jianfei Cai - Nanyang Technological University

S-66 - An Adaptive and Low-Complexity All-Zero Block Detection for HEVC Encoder
Jing Cui{2}, Ruiqin Xiong{2}, Falei Luo{1}, Shanshe Wang{2}, Siwei Ma{2}
{1}Institute of Computing Technology, Chinese Academy of Sciences, China; {2}Peking University, China

S-67 - A Convolutional Neural Network Approach for Half-Pel Interpolation in Video Coding
Ning Yan, Dong Liu, Houqiang Li, Feng Wu
University of Science and Technology of China, China

S-68 - Fast Rate Distortion Optimization with Adaptive Context Group Modeling for HEVC
Hung-Cheng Chen, Tian Sheuan Chang
National Chiao Tung University, Taiwan

S-69 - Fast Rate Distortion Optimized Quantization Method for HEVC
Meng Wang, Xiaodong Xie, Hongfei Fan, Shanshe Wang, Junru Li, Shengfu Dong, Guoqing Xiang, Huizhu Jia
Peking University, China

S-70 - Complexity Reduction by Modes Reduction in RD-List for Intra-Frame Prediction in 3D-HEVC Depth Maps
Gustavo Sanchez{1}, Luciano Agostini{2}, César Marcon{1}
{1}Pontifícia Universidade Católica do Rio Grande do Sul, Brazil; {2}Universidade Federal de Pelotas, Brazil

S-71 - An Efficient Non-Selective Adaptive Motion Compensated Frame Rate Up Conversion
Nguyen Van Thang, Hyuk-Jae Lee
Seoul National University, Korea, South

S-72 - Low-Power and High-Throughput Hardware Design for the 3D-HEVC Depth Intra Skip
Vladimir Afonso{2}, Altamiro Susin{2}, Luan Audibert{1}, Mário Saldanha{1}, Ruhan Conceição{1}, Marcelo Porto{1}, Bruno Zatt{1}, Luciano Agostini{1}
{1}Universidade Federal de Pelotas, Brazil; {2}Universidade Federal do Rio Grande do Sul, Brazil

Complex Networks & Models
Time: Monday, May 29 (15:30-17:00)
Room: Harborside Ballroom
Chair(s): Yoshifumi Nishio - Tokushima University; Federico Bizzarri - Politecnico di Milano

T-73 - Synchronization in Dynamical Oscillatory Networks with Non-Uniform Coupling Distributions
Yoko Uwate, Yoshifumi Nishio
Tokushima University, Japan

T-74 - Multiobjective Transshipment Point Assignment in China Express Delivery Network
Zhongyan Fan, Xiaowen Bi, Doujie Li, Wallace K.S. Tang
City University of Hong Kong, Hong Kong

T-75 - Optimal Design of Coupling Preferences to Mitigate Traffic Congestion in Interconnected Networks
Jian Zhong, Jiajing Wu, Zhenhao Chen, Zibin Zheng
Sun Yat-sen University, China

T-76 - A Unifying Perspective on Phase Noise and Injection Locking
Douglas Frey
Lehigh University, United States

T-77 - Efficient Spectral Graph Sparsification via Krylov-Subspace Based Spectral Perturbation Analysis
Shuhan Zhang{1}, Fan Yang{1}, Xuan Zeng{1}, Dian Zhou{4}, Shun Li{2}, Xiangdong Hu{3}
{1}Fudan University, China; {2}Microsystem & Terahertz Research Center, China; {3}Shanghai High-Performance Integrated-Circuit Design Center, China; {4}University of Texas at Dallas, United States

T-78 - On Network-Based Leader-Following Consensus of Linear Multi-Agent Systems
Lei Ding, Wei Xing Zheng
Western Sydney University, Australia

T-79 - A Heuristics-Based VM Allocation Mechanism for Cloud Data Centers
Jing V. Wang, Nuwan Ganganath, Chi-Tsun Cheng, Chi Kong Tse
Hong Kong Polytechnic University, Hong Kong

T-80 - A Refinement Process for Nozzle Path Planning in 3D Printing
Kai Yin Fok, Chi-Tsun Cheng, Chi Kong Tse
Hong Kong Polytechnic University, Hong Kong

Data Converters II
Time: Monday, May 29 (15:30-17:00)
Room: Harborside Ballroom
Chair(s): Shahriar Mirabbasi - University of British Columbia; George Yuan - Hong Kong University of Science and Technology

U-81 - A Four-Antenna Baseband Multipath Emulator for Millimeter-Wave Channels
Mazen Soliman, Shih-Chang Hung, Jeyanandh Paramesh
Carnegie Mellon University, United States

U-82 - A Low Power Read-Out Circuit with Frequency Accuracy of 0.2% for Capacitive and Resistive Sensors
Qi Peng, Kun Wang, Xuelian Liu, Weifeng Liu, Xiaoming Li, Yiqi Zhuang
Xidian University, China

U-83 - Zero-Bias True Random Number Generator Using LFSR-Based Scrambler
Wei Mao{1}, Yongfu Li{1}, Chun-Huat Heng{1}, Yong Lian{2}
{1}National University of Singapore, Singapore; {2}York University, Canada

U-84 - Piecewise BJT Process Spread Compensation Exploiting Base Recombination Current
Dapeng Sun{2}, Man-Kay Law{2}, Bo Wang{1}, Pui-In Mak{2}, Rui Paulo Martins{2}
{1}Hamad Bin Khalifa University / Hong Kong University of Science and Technology, Qatar; {2}University of Macau, Macau

U-85 - Current Mirror Array: a Novel Lightweight Strong PUF Topology with Enhanced Reliability
Zheng Wang{2}, Yi Chen{1}, Aakash Patil{1}, Chip-Hong Chang{1}, Arindam Basu{1}
{1}Nanyang Technological University, Singapore; {2}Shenzhen Institutes of Advanced Technology, Chinese Academy of Science, China

U-86 - Power Efficient SAR ADC Adaptive to Input Activity for ECG Monitoring Applications
Sungwon Yim, Yujin Park, Han Yang, Suhwan Kim
Seoul National University, Korea, South

U-87 - Nonlinear Quantizer Design in Data Conversion Systems Using the Unscented Transform
José E. G. de Medeiros, Sandro A. P. Haddad
Universidade de Brasília, Brazil

U-88 - A Design-Oriented Approach for Modeling Integrators Non-Idealities in Discrete-Time Sigma-Delta Modulators
Anthony Baltolu{2}, Jean-Baptiste Begueret{1}, Dominique Dallet{1}, Frederic Chalet{2}
{1}IMS Laboratory, France; {2}NXP Semiconductors N.V., France

U-89 - Designing CT Bandpass ΣΔ Modulators with Arbitrary STF Shapes
Johannes Wagner, Jiazuo Chi, Maurits Ortmanns
Universität Ulm, Germany

U-90 - Fundamental Limits on Energy Efficiency Performance of VCO-Based ADCs
John McNeill{2}, Sulin Li{2}, Jianping Gong{2}, Long Pham{1}
{1}Analog Devices Inc., United States; {2}Worcester Polytechnic Institute, United States

U-91 - Digital Interferer Suppression and Jitter Reduction in Continuous-Time Bandpass ΣΔ Modulators
Jiazuo Chi, Johannes Wagner, Jens Anders, Maurits Ortmanns
Universität Ulm, Germany

U-92 - A Novel Clock-Pulse-Width Calibration Technique for Charge Redistribution DACs
Hugo Cruz{1}, Hong-Yi Huang{2}, Ching-Hsing Luo{1}, Lih-Yih Chiou{1}, Shuenn-Yuh Lee{1}
{1}National Cheng Kung University, Taiwan; {2}National Taipei University, Taiwan

U-93 - An 11-Bit 20-MSample/s Pipelined ADC with OTA Bias Current Regulation to Optimize Power Dissipation
Jose Angel Díaz-Madrid{2}, Gines Domenech-Asensi{2}, Jose Alejandro Lopez-Alcantud{2}, Matthias Oberst{1}
{1}Fraunhofer Institute for Integrated Circuits IIS, Germany; {2}Universidad Politécnica de Cartagena, Spain

U-94 - A Digital Compensation Method Canceling Static and Non-Linear Time-Variant Feedback DAC Errors in ΣΔ Analog-to-Digital Converters
Marcel Runge, Friedel Gerfers
Technische Universität Berlin, Germany

***U-95* - A 40 nm CMOS T/H-Less Flash-Like Stroboscopic ADC with 23dB THD and >50 GHz Effective Resolution Bandwidth**
Gibran L. Jaya and Shoushun Chen
Nanyang Technological University, Singapore

U-96 - A Novel High-Rate Hybrid Window ADC Design for Monolithic Digitally-Controlled DC-DC Converters
Yin Sun, Victor Adrian, Joseph Sylvester Chang
Nanyang Technological University, Singapore

Amplifiers, Analog Filtering, RF Circuits & Interface Circuits
Time: Monday, May 29 (15:30-17:00)
Room: Harborside Ballroom
Chair(s): Mohamad Sawan - Polytechnique Montréal; Nuno Paulino – UNINOVA

V-97 - A CMOS Differential-Difference Amplifier with Class-AB Input Stages Featuring Wide Differential-Mode Input Range
Bradley Minch
Franklin W. Olin College of Engineering, United States

V-98 - Offset Based Feedforward Amplifier with Nonlinearity Compensation and P1dB Expansion
Zhan Su{1}, Hossein Noori{1}, Fa Dai{1}, Wei Zhou{2}, Yudong Wang{2}, Jun Fu{2}
{1}Auburn University, United States; {2}Tsinghua University, China

V-99 - A Robust Fully-Dynamic Residue Amplifier for Two-Stage SAR Assisted Pipeline ADCs
Shreya Singh{1}, Pydi Bahubalindruni{1}, João Goes{2}
{1}Indraprastha Institute of Information Technology Delhi, India; {2}Universidade Nova de Lisboa / CTS-UNINOVA, Portugal

V-100 - A Cascode Miller Compensated Three-Stage Amplifier with Local Q-Factor Control for Wide Capacitive Load Applications
Qi Cheng{3}, Weimin Li{1}, Xian Tang{2}, Jianping Guo{1}
{1}Sun Yat-sen University, China; {2}Tsinghua University, China; {3}University of Texas at Dallas, United States

V-101 - A Compact and Low Power Bandpass Amplifier for Low Bandwidth Signal Applications in 65-nm CMOS
Fereidoon Hashemi Noshahr, Mohamad Sawan
Polytechnique Montréal, Canada

V-102 - A 60-GHz Low-Noise Variable-Gain Amplifier in a 130-nm BiCMOS Technology for Sixport Applications
Matthias Völkel, Marco Dietz, Amelie Hagelauer, Robert Weigel, Dietmar Kissinger
Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany

V-103 - A 1.8 µW 32 nV/√Hz Current-Reuse Capacitively-Coupled Instrumentation Amplifier for EEG Detection
Yangtao Dong, Lihan Tang, Xiaolin Yang, Menglian Zhao, Peng Sun, Xiaobo Wu
Zhejiang University, China

V-104 - Linear Input Range Extension for Low-Voltage Operational Transconductance Amplifiers in Gm-C Filters
Mahmoud Ibrahim, Marvin Onabajo
Northeastern University, United States

V-105 - CMOS Mixed Signal SoC for Low-Side Current Sensing
Rahul Thottathil{1}, Veeresh Babu Vulligaddala{1}, Bibhu Datta Sahoo{2}
{1}ams Semiconductors India Pvt Ltd, India; {2}University of Illinois at Urbana-Champaign, United States

V-106 - An Energy/Bandwidth/Area Efficient Frequency-Domain OOK Transmitter with Phase Rotated Modulation
Ranran Zhou, Yining Zhang, Woogeun Rhee, Zhihua Wang
Tsinghua University, China

V-107 - A Class-E RF Power Amplifier with a Novel Matching Network for High-Efficiency Dynamic Load Modulation
Qianqian Liu, Victor Adrian, Bah-Hwee Gwee, Joseph Sylvester Chang
Nanyang Technological University, Singapore

V-108 - A Load Variation Tolerant Readout Interface for High Linear MEMS Capacitive Microphones
Han Yang, Jun Soo Cho, Youngtae Yang, Suhwan Kim
Seoul National University, Korea, South

V-109 - A Widely Tunable Balun Based on 2-Port N-Path Bandpass Filters with Embedded Phase Shifting
Prateek Kumar Sharma, Nagarjuna Nallam
Indian Institute of Technology Guwahati, India

V-110 - A 0.9V 75MHz 2.8mW 4th-Order Analog Filter in CMOS-Bulk 28nm Technology
Fulvio Ciciotti, Marcello De Matteis, Andrea Baschirotto
Università degli Studi di Milano-Bicocca, Italy

V-111 - A Novel Charge Sensitive Pre-Amplifier Structure for Biological Temperature Readout Applications
Hanfeng Wang{2}, Song Yuan{2}, Syed Islam{2}, Charles Britton Jr.{1}
{1}Oak Ridge National Laboratory, United States; {2}University of Tennessee, United States

V-112 - A 0.2V 492nW VCO-Based OTA with 60kHz UGB and 207µVrms Noise
Sarthak Kalani{1}, Alessandro Bertolini{2}, Anna Richelli{2}, Peter R. Kinget{1}
{1}Columbia University, United States; {2}Università degli Studi di Brescia, Italy

V-113 - A High Temperature, 12-Bit-Time-Domain Sensor Interface Based on Injection Locked Oscillator
Emna Chabchoub{1}, Franck Badets{1}, Pascal Nouet{3}, Mohamed Masmoudi{2}, Frédérick Mailly{3}
{1}Commissariat à l'Energie Atomique et aux Energies Alternatives, France; {2}Ecole Nationale d'Ingénieurs de Sfax, Tunisia; {3}Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, France

V-114 - Closed-Loop Continuous-Time Analog Filter with Almost Constant IIP3 Over the Pass-Band
Marcello De Matteis, Antonio D'Amico, Fulvio Ciciotti, Andrea Baschirotto
Università degli Studi di Milano-Bicocca, Italy

Power & Energy Modeling, Analysis, and Design
Time: Monday, May 29 (15:30-17:00)
Room: Harborside Ballroom
Chair(s): Xiaozhe Wang - McGill University; Zbigniew Galias - AGH University of Science and Technology

W-115 - A Multidimensional Transfer Function Model for Frequency Dependent Transmission Lines
Maximilian Schäfer{2}, Rudolf Rabenstein{2}, Christian Strobl{1}
{1}E-T-A Elektrotechnische Apparate GmbH, Germany; {2}Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany

W-116 - A Method to Identify Dynamic Zones for Efficient Control of HVAC Systems
Vinay Kumar, Rakesh Kumar, Deepraj Patkar, Ajit S. Bopardikar
Samsung R&D Institute India, Bangalore, India; Samsung R&D Institute India, Bangalore , India

W-117 - Distributed Optimal Power Flow: an Augmented Lagrangian-Sequential Quadratic Programming Approach
Zejiang Hou, Ho-Chun Wu, Shing-Chow Chan
University of Hong Kong, Hong Kong

W-118 - An FPGA-Based Aperiodic Modulation Strategy for EMI Suppression in Quasi-Z-Source DC-DC Converters
Saad Ul Hasan, Graham E. Town
Macquarie University, Australia

W-119 - On Optimum Placement of Sectionalizing Switches in Radial Distribution Networks
Zbigniew Galias
AGH University of Science and Technology, Poland

W-120 - Dimensioning and Comparison of Common Compensation Topologies for IPT Systems
Martin Trautmann, Marius Ohlendorf, Benedikt Sanftl, Robert Weigel, Alexander Koelpin
Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany

W-121 - Analysis of Coexisting Solutions and Control of Their Bifurcations in a Parallel LC Resonant Inverter
Luis Benadero{2}, Enrique Ponce{1}, Abdelali El Aroudi{3}, Luis Martínez-Salamero{3}
{1}Universidad de Sevilla, Spain; {2}Universitat Politécnica de Catalunya, Spain; {3}Universitat Rovira i Virgili, Spain

W-122 - Stability Conditions for Hybrid Supply Modulators
Min Tan{2}, Wing-Hung Ki{1}
{1}Hong Kong University of Science and Technology, Hong Kong; {2}Huazhong University of Science and Technology, China

W-123 - Dynamic ADC-Quantization for Oscillation-Free Performance of Digitally Controlled Converters
Asif Syed{2}, Amit Patra{1}
{1}Indian Institute of Technology Kharagpur, India; {2}SiWays Microelectronics, India

W-124 - Improving EDP in Multi-Core Embedded Systems Through Multidimensional Frequency Scaling
Wagner Marques{1}, Paulo Souza{1}, Arthur Lorenzon{3}, Antonio Carlos Schneider Beck{3}, Mateus Beck Rutzig{2}, Fábio Rossi{1}
{1}Instituto Federal de Educação, Ciência e Tecnologia Farroupilha, Brazil; {2}Universidade Federal de Santa Maria, Brazil; {3}Universidade Federal do Rio Grande do Sul, Brazil

W-125 - Sliding-Mode Approach for Start-Up Control and Voltage Regulation of a Boost Converter Driving a Constant Power Load
Blanca Areli Martínez-Treviño, Abdelali El Aroudi, Luis Martínez-Salamero
Universitat Rovira i Virgili, Spain

Education Tools
Time: Monday, May 29 (15:30-17:00)
Room: Harborside Ballroom
Chair(s): Yun He - Tsinghua University; Joos Vandewalle - Katholieke Universiteit Leuven

X-126 - An Intrinsic Complexity Model for the Problem of Total Resistance Determination
Abdulhadi Shoufan, Abdulla Alnaqbi
Khalifa University, U.A.E.

X-127 - Using SoC FPAA and Integrated Simulator for Implementation of Circuits and Systems in Education
Aishwarya Natarajan, Jennifer Hasler
Georgia Institute of Technology, United States

X-128 - An Academic EDA Suite for the Full-Custom Design of Mixed-Mode Integrated Circuits
Jofre Pallarès{1}, Keith Sabine{2}, Lluís Terés{1}, Francisco Serra-Graells{1}
{1}Consejo Superior de Investigaciones Científicas, Spain; {2}Peardrop Design Systems Ltd, United Kingdom

PIONEERS OF CAS – MONDAY, MAY 29TH

Pioneers of Circuits and Systems I
Time: Monday, May 29 (17:00-18:00)
Room: Grand Ballroom V-VI
Chair(s): Pamela Abshire - University of Maryland

17:05 ***Distributed Circuit Theory: Reminiscences***
Omar Wing
Columbia University, United States

17:20 ***Present at the Beginning***
Bede Liu
Princeton University, United States

17:35 ***Reminiscence: 60 Years of Teaching Within 84 Years of Life***
Robert Newcomb
University of Maryland, College Park, United States

FUTURECAS PANEL – MONDAY, MAY 29TH

FutureCAS Panel
Time: Monday, May 29 (6:00-7:30)
Room: Grand Ballroom V-VI

What challenges and opportunities does the future hold for the field of Circuits and Systems?
Moderator: Jennifer Blain Christen
Panelists: Jeannette M. Wing, Orla Feely, Mandy Pant, Frederica Darema

Radar Circuits and Systems
Time: Tuesday, May 30 (8:00-9:30)
Room: Dover A
Chair(s): Ioannis Syllaios - University of Texas at Dallas; Joseph Chang - Nanyang Technological University

8:00 ***Time-of-Arrival Measurement Using Adaptive CMOS IR-UWB Range Finder with Scalable Resolution***
Tae Hwan Jin{1}, Hong Gul Han{2}, Tae Wook Kim{2}
{1}Samsung Electronic, Korea, South; {2}Yonsei University, Korea, South

8:18 ***Real-Time Mitigation of Short-Range Leakage in Automotive FMCW Radar Transceivers***
Alexander Melzer{2}, Mario Huemer{2}, Florian Starzer{1}, Herbert Jäger{1}
{1}DICE GmbH & Co KG, Austria; {2}Johannes Kepler Universität Linz, Austria

8:36 ***Novel Mixed-Signal Based Short-Range Leakage Canceler for FMCW Radar Transceiver MMICs***
Alexander Melzer{2}, Mario Huemer{2}, Alexander Onic{1}
{1}DICE Danube Integrated Circuit Engineering GmbH & Co. KG, Austria; {2}Johannes Kepler Universität Linz, Austria

8:54 ***Modeling and Analysis of the Effects of PLL Phase Noise on FMCW Radar Performance***
Debashis Dhar{1}, P.T.M. van Zeijl{2}, Dusan Milosevic{1}, Hao Gao{1}, Arthur H. M. van Roermund{1}
{1}Eindhoven University of Technology, Netherlands; {2}Omniradar BV, Netherlands

9:12 ***A Dual Band FMCW Radar Receiver with Integrated Active Balun and Baseband AGC Loop***
Mohammed El-Shennawy, Belal Al-Qudsi, Niko Joram, Frank Ellinger
Technische Universität Dresden, Germany

IoVT Panel
Time: Tuesday, May 30 (8:00-9:30)
Room: Dover BC
Moderator(s): Dr. Yen-Kuang Chen - Intel Corporation, Prof. Eduard Alarcon - UPC

Deep Learning for Internet of Video Things – Hype or Hope?
Panelists:
Prof. Magdy Bayoumi, University of Louisiana at Lafayette, USA
Prof. Shao-Yi Chien, National Taiwan University, USA
Dr. Shipeng Li, Cogobuy/IngDan, China
Prof. Yung-Hsiang Lu, Purdue University, USA
Prof. Tokunbo Ogunfunmi, Santa Clara University, USA

Hardware Accelerators for Deep Learning & Cognitive Systems
Time: Tuesday, May 30 (8:00-9:30)
Room: Grand Ballroom I
Chair(s): Ralph Etienne-Cummings - Johns Hopkins University; Chetan Thakur - Johns Hopkins University

8:00 ***Fast Classification Using Sparsely Active Spiking Networks***
Hesham Mostafa, Bruno Pedroni, Sadique Sheik, Gert Cauwenberghs
University of California, San Diego, United States

8:18 ***A Fixed Point Exponential Function Accelerator for a Neuromorphic Many-Core System***
Johannes Partzsch{1}, Sebastian Höppner{1}, Matthias Eberlein{1}, Rene Schüffny{1}, Christian Mayr{1}, David R. Lester{2}, Steve Furber{2}
{1}Technische Universität Dresden, Germany; {2}University of Manchester, United Kingdom

8:36 ***Event-Driven Random Backpropagation: Enabling Neuromorphic Deep Learning Machines***
Emre Neftci{2}, Charles Augustine{1}, Somnath Paul{1}, Georgios Detorakis{2}
{1}Intel Corporation, United States; {2}University of California, Irvine, United States

8:54 ***Pattern Representation and Recognition with Accelerated Analog Neuromorphic Systems***
Mihai Alexandru Petrovici{2}, Sebastian Schmitt{2}, Johann Klähn{2}, David Stöckel{2}, Anna Schroeder{2}, G. Bellec{4}, Johannes Bill{2}, Oliver Breitwieser{2}, Ilja Bytschok{2}, Andreas Grübl{2}, Maurice Güttler{2}, Andreas Hartel{2}, Stephan Hartmann{3}, Dan Husmann{2}, Kai Husmann{2}, S. Jeltsch{2}, Vitali Karasenko{2}, M. Kleider{2}, C. Koke{2}, A. Kononov{2}, C. Mauch{2}, P. Müller{2}, Johannes Partzsch{3}, T. Pfeil{2}, Stefan Schiefer{3}, Stefan Scholze{3}, A. Subramoney{1}, V. Thanasoulis{3}, Bernhard Vogginger{3}, Robert Legenstein{1}, Wolfgang Maass{1}, Rene Schüffny{3}, Christian Mayr{3}, Johannes Schemmel{2}, Karlheinz Meier{2}
{1}Graz University of Technology, Austria; {2}Ruprecht-Karls-Universität Heidelberg, Germany; {3}Technische Universität Dresden, Germany; {4}Technische Universität Graz, Germany

9:12 ***Ziksa: on-Chip Learning Accelerator with Memristor Crossbars for Multilevel Neural Networks***
Abdullah M. Zyarah{1}, Nicholas Soures{1}, Lydia Hays{1}, Robin Jacobs-Gedrim{2}, Sapan Agarwal{2}, Matthew Marinella{2}, Dhireesha Kudithipudi{1}
{1}Rochester Institute of Technology, United States; {2}Sandia National Laboratories, United States

Compressive Sensing
Time: Tuesday, May 30 (8:00-9:30)
Room: Grand Ballroom II
Chair(s): Wei-Ping Zhu - Concordia University; Yun Chen - Fudan University

8:00 ***Countering the False Myth of Democracy: Boosting Compressed Sensing Performance with Maximum-Energy Approach***
Mauro Mangia{2}, Fabio Pareschi{1}, Riccardo Rovatti{2}, Gianluca Setti{1}
{1}Università degli Studi di Ferrara, Italy; {2}Università di Bologna, Italy

8:18 ***Subspace Learning in the Presence of Sparse Structured Outliers and Noise***
Shervin Minaee, Yao Wang
New York University, United States

8:36 ***Scaled Linearized Bregman Iterations for Fixed Point Implementation***
Michael Lunglmayr, Bernhard Hiptmair, Mario Huemer
Johannes Kepler Universität Linz, Austria

8:54 ***Two-Pass Lp-Regularized Least-Squares Algorithm for Compressive Sensing***
Jeevan Pant, Sridhar Krishnan
Ryerson University, Canada

9:12 ***Approximate-DCT-Derived Measurement Matrices for Compressed Sensing***
Jianbin Zhou, Dajiang Zhou, Yoshimura Takeshi, Satoshi Goto
Waseda University, Japan

Circuits for Power Management & Voltage References
Time: Tuesday, May 30 (8:00-9:30)
Room: Grand Ballroom III
Chair(s): Nathan Neihart - Iowa State University; Jose Silva-Martinez - Texas A&M University

8:00 ***A Power-Efficient Reconfigurable Output-Capacitor-Less Low-Drop-Out Regulator for Low Power Analog Sensing Front-End***
Sheng-Yu Peng, Li-Han Liu, Pei-Ke Chang, Tzu-Yun Wang, Hao-Yu Li
National Taiwan University of Science and Technology, Taiwan

8:18 ***An All-MOSFET Sub-1 V Voltage Reference with a - 51 dB PSR Up to 60 MHz***
Nashiru Alhassan{1}, Edgar Sánchez-Sinencio{1}, Zekun Zhou{2}
{1}Texas A&M University, United States; {2}Texas A&M University / University of Electronic Science and Technology of China, United States

8:36 ***An All-MOSFET Voltage Reference with -50dB PSR @ 80 MHz for Low Power SoC Design***
Nashiru Alhassan{1}, Edgar Sánchez-Sinencio{1}, Zekun Zhou{2}
{1}Texas A&M University, United States; {2}Texas A&M University / University of Electronic Science and Technology of China, United States

8:54 ***A Simple LDO with Adaptable Bias for Internet of Things Applications***
Igor Filanovsky{4}, Luis Bica Oliveira{3}, Nikolay Tchamov{1}, Vadim Ivanov{2}
{1}Tampere University of Technology, Finland; {2}Texas Instruments Inc., United States; {3}Universidade Nova de Lisboa, Portugal; {4}University of Alberta, Canada

Hardware Security
Time: Tuesday, May 30 (8:00-9:30)
Room: Grand Ballroom IV
Chair(s): Ankur Srivastava - University of Maryland; Chip Hong Chang - Nanyang Technological University

8:00 ***A Voltage Regulator-Assisted Lightweight AES Implementation Against DPA Attacks***
Weize Yu, Selcuk Köse
University of South Florida, United States

8:18 ***CPA Secured Data-Dependent Delay-Assignment Methodology***
Itamar Levi, Osnat Keren, Alexander Fish
Bar-Ilan University, Israel

8:36 ***CMOS Based Gates for Blurring Power Information***
Moshe Avital, Itamar Levi, Osnat Keren, Alexander Fish
Bar-Ilan University, Israel

8:54 ***Charge-Withheld Converter-Reshuffling (CoRe): a Countermeasure Against Power Analysis Attacks***
Weize Yu, Selcuk Köse
University of South Florida, United States

Vision Sensors
Time: Tuesday, May 30 (8:00-9:30)
Room: Grand Ballroom VII
Chair(s): Piotr Dudek - The University of Manchester; Ricardo Carmona Galán - Instituto of Microelectrónica of Sevilla

8:00 ***INVITED: Development of an Always-on Vision Computer Vision Sensor***
Venkat Rangan
Qualcomm Inc., United States

8:18 ***Always-on CMOS Image Sensor Pixel Design for Pixel-Wise Binary Coded Exposure***
Yi Luo
University of British Columbia., Canada

8:36 ***A Dynamic Vision Sensor with Direct Logarithmic Output and Full-Frame Picture-on-Demand***
Jing Huang, Menghan Guo, Shoushun Chen
Nanyang Technological University, Singapore

8:54 ***Impact of Fixed Pattern Noise on Embedded Image Compression Techniques***
William Guicquero, Laurent Alacoque
Commissariat à l'Energie Atomique et aux Energies Alternatives, France

9:12 ***High-Speed Depth from Focus on a Programmable Vision Chip Using a Focus Tunable Lens***
Julien N.P. Martel{1}, Lorenz K. Müller{1}, Stephen J. Carey{2}, Piotr Dudek{2}
{1}Universität Zürich / Eidgenössische Technische Hochschule Zürich, Switzerland; {2}University of Manchester, United Kingdom

Digitally Intensive Frequency Synthesis for Internet of Things Applications
Time: Tuesday, May 30 (8:00-8:30)
Room: Grand Ballroom VIII
Chair(s): Paul Sotiriadis - University of California, San Diego; Peter Kennedy - University College Cork

8:00 ***Analysis of Millimeter-Wave Digital Frequency Modulators for Ubiquitous Sensors and Radars***
Dmytro Cherniak{3}, Salvatore Levantino{2}, Carlo Samori{2}, Roberto Nonis{1}
{1}Infineon Technologies, Austria; {2}Politecnico di Milano, Italy; {3}Politecnico di Milano / Infineon, Italy

8:18 ***All Digital FPGA-Implementable Time-Average-Frequency Direct Period Synthesis for IoT Applications***
Liming Xiu
BOE Technology Group CO., LTD., China

8:36 ***Hybrid-DPLL-Based Constant-Envelope Modulator for Internet-of-Things Chipsets***
Ioannis Syllaios
Cypress Semiconductor, United States

8:54 ***Single-Bit All Digital Frequency Synthesis with Homodyne Sigma-Delta Modulation for Internet of Things Applications***
Paul Peter Sotiriadis, Charis Basetas
National Technical University of Athens, Greece

9:12 ***Nonlinearity-Induced Spurious Tones and Noise in Digitally-Assisted Frequency Synthesizers***
Michael Peter Kennedy, Hongjia Mo, Dawei Mai
University College Cork, Ireland

Wireless & Implantable/Injectable Technology Circuits & Systems II
Time: Tuesday, May 30 (8:00-9:30)
Room: Grand Ballroom IX
Chair(s): Shantanu Chakrabartty - Washington University in St. Louis; Benoit Gosselin - Université Laval

8:00 ***A CMOS Automatic Tuning System to Maximize Remote Powering Efficiency***
Paul Gosselin{1}, Roberto Puddu{2}, Alexis Carreira{1}, Mehrdad Ghanad{1}, Massimo Barbaro{2}, Catherine Dehollain{1}
{1}École Polytechnique Fédérale de Lausanne, Switzerland; {2}Università degli Studi di Cagliari, Italy

8:18 ***Feasibility of Hybrid Ultrasound-Electrical Nerve Stimulation for Electroceuticals***
Brittany Scheid, Shantanu Chakrabartty
Washington University in St. Louis, United States

8:36 ***A High-Sensitivity CMOS Biophotometry Sensor with Embedded Continuous-Time ΣΔ Modulation***
Mehdi Noormohammadi Khiarak{2}, Sylvain Martel{1}, Yves De Koninck{2}, Benoit Gosselin{2}
{1}Polytechnique Montréal, Canada; {2}Université Laval, Canada

8:54 ***In-Vivo Tests of an Inductively Powered Miniaturized Neural Stimulator***
Adam Khalifa{1}, Yasha Karimi{3}, Qihong Wang{1}, Elliot Greenwald{1}, Sherry Chiu{1}, Milutin Stanaćević{3}, Nitish Thakor{2}, Ralph Etienne-Cummings{1}
{1}Johns Hopkins University, United States; {2}Johns Hopkins University / National University of Singapore, United States; {3}Stony Brook University, United States

9:12 ***Towards Low-Power Wearable Wireless Sensors for Molecular Biomarker and Physiological Signal Monitoring***
Xueyuan Zhao, Vidyasagar Sadhu, Tuan Le, Dario Pompili, Mehdi Javanmard
Rutgers University, United States

ADCs for Wireless Communication
Time: Tuesday, May 30 (8:00-9:30)
Room: Grand Ballroom X
Chair(s): Thierry Taris - Laboratoire de l'Intégration du Matériau au Système; Joseph Chang - Nanyang Technological University

8:00 ***Mismatch-Shaped Frequency-Interleaved Quadrature Data Converters for Carrier Aggregation in MU-MIMO***
Sandipan Kundu{2}, Subhanshu Gupta{3}, David Allstot{3}, Jeyanandh Paramesh{1}
{1}Carnegie Mellon University, United States; {2}Intel Corporation, United States; {3}Washington State University, United States

8:18 ***An Adaptive Blind Frequency Response Mismatches Calibration Method for Four-Channel TIADCs Based on Channel Swapping***
Husheng Liu, Hui Xu
National University of Defense Technology, China

8:36 ***A 5-Bit 300–900-MS/s 0.8–1.2-V Supply Voltage ADC with Background Self-Calibration***
Fábio Alex Rabuske{2}, Taimur Gibran Rabuske{1}, Jorge Fernandes{2}
{1}Instituto de Engenharia de Sistemas e Computadores - Investigação e Desenvolvimento, Portugal; {2}Universidade Técnica de Lisboa / Instituto de Engenharia de Sistemas e Computadores - Investigação , Portugal

8:54 ***A 7.9µA 4-Bit 4Msps Successive Approximation Phase-Domain ADC for GFSK Demodulator***
Shaoquan Gao, Hanjun Jiang, Zhaoyang Weng, Yanshu Guo, Jingjing Dong, Zhihua Wang
Tsinghua University, China

9:12 ***A Two-Step Radio Receiver Architecture Fully Embedded Into a Charge-Sharing SAR ADC***
Nuno Pereira, Hugo Serra, João Goes
Universidade Nova de Lisboa / CTS-UNINOVA, Portugal

Cognitive Radio & Security Systems
Time: Tuesday, May 30 (8:00-9:30)
Room: Laurel AB
Chair(s): Maire O'Neill - Queens University; Joseph Cavallaro - Rice University

8:00 ***INVITED: Hardware Security at the Heart of IoT***
Mathias Wagner
NXP Semiconductors N.V., United States

8:18 ***Computational Complexity Reduction for Signal Cyclostationarity Detection Based Spectrum Sensing***
Shuske Narieda
National Institute of Technology, Akashi College, Japan

8:36 ***A 3DES Implementation Especially for CBC Feedback Loop Mode***
Yongcheng He, Shuguo Li
Tsinghua University, China

8:54 ***Compact and Provably Secure Lattice-Based Signatures in Hardware***
James Howe, Ciara Rafferty, Ayesha Khalid, Maire O'Neill
Queen's University Belfast, United Kingdom

9:12 ***A Sub-mW Spectrum Sensing Architecture for Portable IEEE 802.22 Cognitive Radio Applications***
Kevin Banović, Anthony Chan Carusone
University of Toronto, Canada

Arithmetic & Logic Circuits
Time: Tuesday, May 30 (8:00-9:30)
Room: Laurel CD
Chair(s): Ettore Napoli - Università degli Studi di Napoli Federico II; Martin Kumm - Universität Kassel

8:00 ***Analysis of Stochastic Logic Circuits in Unipolar, Bipolar and Hybrid Formats***
Keshab K. Parhi
University of Minnesota Twin Cities, United States

8:18 ***Logarithmic Number System Addition-Subtraction Using Fractional Normalization***
Giorgos Tsiaras, Vassilis Paliouras
University of Patras, Greece

8:36 ***Post-Processing of Supergate Networks Aiming Cell Layout Optimization***
Gustavo Smaniotto{2}, Regis Zanandrea{2}, Maicon Cardoso{2}, Renato de Souza{2}, Matheus Moreira{1}, Felipe Marques{2}, Leomar Da Rosa Jr.{2}
{1}Pontifícia Universidade Católica do Rio Grande do Sul, Brazil; {2}Universidade Federal de Pelotas, Brazil

8:54 ***Integration of Level Shifting in a TSPC Flip-Flop for Low-Power Robust Timing Closure in Dual-VDD ULV Circuits***
François Stas, David Bol
Université Catholique de Louvain, Belgium

9:12 ***Cell Spreading Optimization for Force-Directed Global Placers***
Xueyan Wang, Yici Cai, Qiang Zhou
Tsinghua University, China

Advanced Video Streaming & Transmission
Time: Tuesday, May 30 (8:00-9:30)
Room: Kent AB
Chair(s): Hsu-Feng Hsiao - National Chiao Tung University; Jianfei Cai - Nanyang Technological University

8:00 ***Collaborative Wireless Freeview Video Streaming with Network Coding***
Bo Zhang{4}, Zhi Liu{3}, S.-H. Gary Chan{1}, Gene Cheung{2}
{1}Hong Kong University of Science and Technology, Hong Kong; {2}National Institute of Informatics, Japan; {3}Waseda University, Japan; {4}Zhengzhou University, China

8:18 ***Dynamic Threshold Based Rate Adaptation for HTTP Live Streaming***
Lan Xie, Chao Zhou, Xinggong Zhang, Zongming Guo
Peking University, China

8:36 ***View Direction and Bandwidth Adaptive 360 Degree Video Streaming Using a Two-Tier System***
Fanyi Duanmu, Eymen Kurdoglu, Yong Liu, Yao Wang
New York University, United States

8:54 ***A Robust Video Encoding Scheme to Enhance Error Concealment of Intra Frames***
Joao Carreira{1}, Pedro Assuncao{1}, Sergio Faria{1}, Erhan Ekmekcioglu{2}, Ahmet Kondoz{2}
{1}Intituto deTelecomunicacoes, Portugal; {2}Loughborough University London, United Kingdom

9:12 ***Video Streaming Optimization Using Degradation Estimation with Unequal Error Protection***
Philip Tovstogan, Hsu-Feng Hsiao
National Chiao Tung University, Ukraine; National Chiao Tung University, Taiwan

Mini-Tutorial
Time: Tuesday, May 30 (8:00-9:30)
Room: Essex AB

Multiply and Filter: An Universal Measurement Trick
Arijit Sinharay
Innovation Lab, Kolkata, India

Keynote
Time: Tuesday, May 30 (9:30-10:30)
Room: Grand Ballroom V-VI

A Matter of Trust
Kerry Bernstein, Program Manager, Microsystems Technology Office, DARPA

Nonlinear Dynamics in CAS
Time: Tuesday, May 30 (11:00-12:30)
Room: Dover A
Chair(s): Marco Storace - Università di Genova; Dimitri Galayco - Université Pierre-et-Marie-Curie

11:00 ***Control-Oriented Design Guidelines to Extend the Stability Margin of Switching Converters***
Kuntal Mandal{3}, Abdullah Abusorrah{2}, Mohammed M. Al-Hindawi{2}, Yusuf Al-Turki{2}, Abdelali El Aroudi{4}, Damian Giaouris{5}, Soumitro Banerjee{1}
{1}Indian Institute of Science Education and Research, Kolkata, India; {2}King Abdulaziz University, Saudi Arabia; {3}National Institute of Technology Sikkim, India; {4}Universitat Rovira i Virgili, Spain; {5}University of Newcastle, United Kingdom

11:18 ***A Modified CCM Approach for Simulating Hierarchical Interconnected Dynamical Systems***
Michael Popp, Wolfgang Mathis, Malte John, Olga Korolova, Axel Mertens, Bernd Ponick
Gottfried Wilhelm Leibniz Universität Hannover, Germany

11:36 ***CEPAGE: a Toolbox for Central Pattern Generator Analysis***
Matteo Lodi{2}, Andrey Shilnikov{1}, Marco Storace{2}
{1}Georgia State University, United States; {2}Università di Genova, Italy

11:54 ***Constant-Time Discontinuity Map for Forward Sensitivity Analysis to Initial Conditions: Spurs Detection in Fractional-N PLL as a Case Study***
Federico Bizzarri{1}, Angelo Brambilla{1}, Alessandro Colombo{1}, Sergio Callegari{2}
{1}Politecnico di Milano, Italy; {2}Università di Bologna, Italy

12:12 ***Semianalytical Model for High Speed Analysis of All-Digital PLL Clock-Generating Networks***
Eugene Koskin{2}, Dimitri Galayko{1}, Orla Feely{2}, Elena Blokhina{2}
{1}Laboratoire d'informatique de Paris 6 / Université Pierre et Marie Curie / Sorbonne Universités, France; {2}University College Dublin, Ireland

Power Converters I
Time: Tuesday, May 30 (11:00-12:30)
Room: Dover BC
Chair(s): Abdelali El Aroudi - Universitat Rovira i Virgili; Hiroo Sekiya - Chiba University

11:00 ***A Low-Voltage Charge Pump with Improved Pumping Efficiency***
Xiaoxue Jiang, Xiaojian Yu, Jie Chen
University of Alberta, Canada

11:18 ***Modeling of 3-Level Buck Converters in Discontinuous Conduction Mode for Stand-by Mode Power Supply***
Yoshitaka Yamauchi, Toru Sai, Takayasu Sakurai, Makoto Takamiya
University of Tokyo, Japan

11:36 ***A Class-D Output Bridge with Dynamic Dead-Time, Small Delay and Reduced EMI***
Timucin Karaca, Mario Auer
Graz University of Technology, Austria

11:54 ***A Current Average Control Method for Transient-Glitch Reduction in Variable Frequency DC-DC Converters***
Hsin-Shu Chen, Jia-Nan Tai, Yi-Jan Emery Chen, Jau-Horng Chen
National Taiwan University, Taiwan

12:12 ***A Novel Nonlinear Modulation Technique for Stabilizing DC-DC Switching Converters***
Abdelali El Aroudi{4}, Kuntal Mandal{3}, Abdullah Abusorrah{2}, Mohammed M. Al-Hindawi{2}, Yusuf Al-Turki{2}, Damian Giaouris{5}, Soumitro Banerjee{1} {1}Indian Institute of Science Education and Research, Kolkata, India; {2}King Abdulaziz University, Saudi Arabia; {3}National Institute of Technology Sikkim, India; {4}Universitat Rovira i Virgili, Spain; {5}University of Newcastle, United Kingdom

Pattern Recognition & Learning Systems I
Time: Tuesday, May 30 (11:00-12:30)
Room: Grand Ballroom I
Chair(s): Ibrahim Elfadel - Masdar Institute; Jeremy Holleman - University of North Carolina at Charlotte

11:00 ***INVITED: Using Machine Learning to Separate Signals***
Peder Olsen
IBM Research, United States

11:18 ***Accelerating Convolutional Neural Network with FFT on Tiny Cores***
Tahmid Abtahi, Amey Kulkarni, Tinoosh Mohsenin
University of Maryland, Baltimore County, United States

11:36 ***A Mixed-Mode Array Computing Architecture for Online Dictionary Learning***
Jussi Poikonen, Mika Laiho
University of Turku, Finland

11:54 ***VLSI Implementation of LS-SVM Training and Classification Using Entropy Based Subset-Selection***
Andreas Bytyn, Jannik Springer, Rainer Leupers, Gerd Ascheid
Rheinisch-Westfälische Technische Hochschule Aachen, Germany

12:12 ***Fast Thermopile Readout Circuit Arrangement for Array Processors***
Mika Grönroos, Tapani Nevalainen, Jonne Poikonen, Ari Paasio
University of Turku, Finland

Statistical Signal Processing
Time: Tuesday, May 30 (11:00-12:30)
Room: Grand Ballroom II
Chair(s): Wei Xing Zheng - Western Sydney University; Tokunbo Ogunfunmi - Santa Clara University

11:00 ***Efficient Data Structures for Density Estimation for Large High-Dimensional Data***
Aref Majdara, Saeid Nooshabadi
Michigan Technological University, United States

11:18 ***Integer Frequency Offset Detection with Reduced Complexity in OFDM Systems***
Hamed Abdzadeh-Ziabari, Wei-Ping Zhu, M.N.S. Swamy
Concordia University, Canada

11:36 ***A New Regularized Recursive Dynamic Factor Analysis with Variable Forgetting Factor for Wireless Sensor Networks with Missing Data***
Jian-Qiang Lin, Ho-Chun Wu, Shing-Chow Chan
University of Hong Kong, Hong Kong

11:54 ***Study of Wind Profile Prediction with a Combination of Signal Processing and Computational Fluid Dynamics***
Mengdi Jiang, Wei Liu, Yi Li
University of Sheffield, United Kingdom

12:12 ***Multichannel Color Image Watermark Detection Utilizing Vector-Based Hidden Markov Model***
Marzieh Amini, Hamidreza Sadreazami, M. Omair Ahmad, M.N.S. Swamy
Concordia University, Canada

RF Circuits I
Time: Tuesday, May 30 (11:00-12:30)
Room: Grand Ballroom III
Chair(s): Joseph Chang - Nanyang Technological University; Ioannis Syllaios - University of Texas at Dallas

11:00 ***A 30µW, 3.3dB NF CMOS LNA for Wearable WSN Applications***
Ehsan Kargaran, Danilo Manstretta, Rinaldo Castello
Università degli Studi di Pavia, Italy

11:18 ***A 6V CMOS Switching Mode Amplifier for Continuous-Wave Signals from DC to 3 GHz***
Robert Bieg, Martin Schmidt, Markus Grözing, Manfred Berroth
Universität Stuttgart, Germany

11:36 ***Common-Mode Termination Requirements in Concurrent Dual-Band Push-Pull Power Amplifiers***
Byron Montgomery, Yifei Li, Nathan Neihart
Iowa State University, United States

11:54 ***A 1024-QAM Capable WLAN Receiver with -56.3 dB Image Rejection Ratio Using Self-Calibration Technique***
Shusuke Kawai, Toshiyuki Yamagishi, Yosuke Hagiwara, Shigehito Saigusa, Ichiro Seto, Shoji Otaka, Shuichi Ito
Toshiba Corporation, Japan

12:12 ***Impact of Amplifier Bandwidth Limitations on Gain-Boosted N-Path Receivers***
Debasish Mitra{1}, Dusan Milosevic{1}, Salvatore Drago{2}, Jan van Sinderen{2}, Lucien J. Breems{2}
{1}Eindhoven University of Technology, Netherlands; {2}NXP Semiconductors N.V., Netherlands

Intellectual Property Protection: A special session in honor of Professor Miodrag Potkonjak
Time: Tuesday, May 30 (11:00-12:30)
Room: Grand Ballroom IV
Chair(s): Gang Qu - University of Maryland

11:00 ***20 Years of Research on Intellectual Property Protection***
Miodrag Potkonjak{2}, Gang Qu{4}, Farinaz Koushanfar{3}, Chip-Hong Chang{1}
{1}Nanyang Technological University, Singapore; {2}University of California, Los Angeles, United States; {3}University of California, San Diego, United States; {4}University of Maryland, College Park, United States

11:18 ***INVITED: Cybersecurity and the Electric Grid: Innovation and Intellectual Property***
Theodore Wood{2}, Marc Dandin{1}
{1}Wood IP LLC, United States; {2}Wood IP LLC , United States

11:36 ***Practical IP Watermarking and Fingerprinting Methods for ASIC Designs***
Xi Chen{2}, Gang Qu{2}, Aijiao Cui{1}
{1}Harbin Institute of Technology, China; {2}University of Maryland, College Park, United States

11:54 ***Hardware-Based Anti-Counterfeiting Techniques for Safeguarding Supply Chain Integrity***
Md Tanvir Arafin{2}, Andrew Stanley{1}, Praveen Sharma{1}
{1}Koninklijke Philips N.V., United States; {2}University of Maryland, College Park, United States

12:12 ***Revisit Sequential Logic Obfuscation: Attacks and Defenses***
Travis Meade{1}, Zheng Zhao{2}, Shaojie Zhang{1}, David Pan{2}, Yier Jin{1}
{1}University of Central Florida, United States; {2}University of Texas at Austin, United States

Sensing Circuits
Time: Tuesday, May 30 (11:00-12:30)
Room: Grand Ballroom VII
Chair(s): Meng-Fan Chang - National Tsing Hua University; Joseph Friedman - University of Texas at Dallas

11:00 ***From "MISSION: IMPOSSIBLE" to Mission Possible: Fully Flexible Intelligent Contact Lens for Image Classification with Analog-to-Information Processing***
Qin Li{2}, Zheyu Liu{2}, Fei Qiao{2}, Xing Wu{1}, Chaolun Wang{1}, Qi Wei{2}, Huazhong Yang{2}
{1}East China Normal University, China; {2}Tsinghua University, China

11:18 ***FPGA-Based Neural Probe Positioning to Improve Spike Sorting with OSort Algorithm***
László Schäffer{3}, Zoltán Nagy{2}, Zoltán Kincses{3}, Richárd Fiáth{1}
{1}Hungarian Academy of Sciences, Hungary; {2}Pázmány Peter Catholic University, Hungary; {3}University of Szeged, Hungary

11:36 ***A Novel ISFET Sensor Architecture Using Through-Silicon Vias for DNA Sequencing***
Wei Xiao, Nicholas Miscourides, Pantelis Georgiou
Imperial College London, United Kingdom

11:54 ***Behaving Cyborg Locusts for Standoff Chemical Sensing***
Darshit Mehta, Ege Altan, Rishabh Chandak, Baranidharan Raman, Shantanu Chakrabartty
Washington University in St. Louis, United States

12:12 ***A Modular Wireless Sensor Platform and its Applications***
Chun-Ming Huang, Yi-Jie Hsieh, Wei-Lin Lai, Yi-Jun Liu, Chun-Ying Juan, Ssu-Ying Chen, Chun-Yu Chen, Jin-Ju Chue, Chih-Chyau Yang, Chien-Ming Wu
National Applied Research Laboratories, Taiwan

Flexible-Hybrid & Printable Electronics Systems
Time: Tuesday, May 30 (11:00-12:30)
Room: Grand Ballroom VIII
Chair(s): Fayomi Christian - Université du Québec à Montréal; Gordon Roberts - McGill University

11:00 ***Printed Electronics: Effects of Bending and a Self-Compensation Means***
Jia Zhou, Tong Ge, Joseph Sylvester Chang
Nanyang Technological University, Singapore

11:18 ***Flexible Hydrogel Actuated Graphene-Cellulose Biosensor for Monitoring Ph***
George Knopf, Dogan Sinar
University of Western Ontario, Canada

11:36 ***Review: a Fully-Additive Printed Electronics Process with Very-Low Process Variations (Bent and Unbent Substrates) and PDK***
Tong Ge, Jia Zhou, Yang Kang, Joseph Sylvester Chang
Nanyang Technological University, Singapore

11:54 ***Powering Smart Wearable Systems with Flexible Solar Energy Harvesting***
Petar Jokic, Michele Magno
Eidgenössische Technische Hochschule Zürich, Switzerland

12:12 ***Towards a Smartphone-Aided Electronic ELISA for Real-Time Electrochemical Monitoring***
Nikolaos Pechlivanidis, Konstantinos Papadimitriou, Daniel Evans, Nikolaos Vasilakis, Themistoklis Prodromakis
University of Southampton, United Kingdom

CAS for Human Machine Interfaces / Brain Machine Interfaces
Time: Tuesday, May 30 (11:00-12:30)
Room: Grand Ballroom IX
Chair(s): Julius Georgiou - University of Cyprus; Pantelis Georgiou - Imperial College London

11:00 ***A High Temporal Resolution Multiscale Recording System for in Vivo Neural Studies***
Gian Nicola Angotzi{2}, Mario Malerba{2}, Alessandro Maccione{2}, Fabio Boi{2}, Marco Crepaldi{2}, Alberto Bonanno{1}, Luca Berdondini{2}
{1}Istituto Italiano di Tecnolgia, Italy; {2}Istituto Italiano di Tecnologia, Italy

11:18 ***A Silicon Based fdNIRS System with Integrated tDCS on Chip for Non-Invasive Closed-Loop Neuro Stimulation***
Yun Miao, Valencia Koomson
Tufts University, United States

11:36 ***A Fully Integrated Wireless Sensor-Brain Interface System to Restore Finger Sensation***
Xilin Liu{2}, Hongjie Zhu{2}, Milin Zhang{1}, Xiaotie Wu{1}, Andrew Richardson{2}, Srihari Sritharan{2}, Dengteng Ge{2}, Yang Shu{2}, Timothy Lucas{2}, Jan Van der Spiegel{2}
{1}Tsinghua University, China; {2}University of Pennsylvania, United States

11:54 ***A Charge-Based Ultra-Low Power Continuous-Time ADC for Data Driven Neural Spike Processing***
Michal Maslik{1}, Yan Liu{1}, Tor Sverre Lande{2}, Timothy Constandinou{1}
{1}Imperial College London, United Kingdom; {2}University of Oslo, Norway

12:12 ***Analysis of Passive Charge Balancing for Safe Current-Mode Neural Stimulation***
Luis Eduardo Rueda Guerrero{2}, Marco Ballini{1}, Nick Van Helleputte{1}, Srinjoy Mitra{3}
{1}IMEC, Belgium; {2}Universidad Industrial de Santander, Colombia; {3}University of Glasgow, United Kingdom

Data Converters I
Time: Tuesday, May 30 (11:00-12:30)
Room: Grand Ballroom X
Chair(s): Ioannis Syllaios - University of Texas at Dallas; George Yuan - Hong Kong University of Science and Technology

11:00 ***A Novel Wavelet-Based Analog-to-Digital Converter***
Isadora Freire Martins{2}, José Edil Guimarães de Medeiros{2}, José Alberto Alves de Andrade{1}, Sandro Augusto Pavlik Haddad{2}
{1}DFchip Ltd., Brazil; {2}Universidade de Brasília, Brazil

11:18 ***Voltage Domain Correction Technique for Timing Skew Errors in Time Interleaved ADCs***
Praveen Kumar Venkatachala{1}, Ahmed Elshater{1}, Yang Xu{1}, Manar El-Chammas{2}, Un-Ku Moon{1}
{1}Oregon State University, United States; {2}Texas Instruments Inc., United States

11:36 ***A 700µW 1GS/s 4-Bit Folding-Flash ADC in 65nm CMOS for Wideband Wireless Communications***
Bayan Nasri, Sunit Sebastian, Kae-Dyi You, Ramkumar RanjithKumar, Davood Shahrjerdi
New York University, United States

11:54 ***A Highly Linear OTA-Free VCO-Based 1-1 MASH ΔΣ ADC***
Hamidreza Maghami{2}, Pedram Payandehnia{2}, Hossein Mirzaie{2}, Kartikeya Mayaram{2}, Ramin Zanbaghi{1}, Terri Fiez{3}
{1}Cirrus logic, United States; {2}Oregon State University, United States; {3}University of Colorado Boulder, United States

12:12 ***Thermal Noise Canceling Pipelined ADC***
Chithira Ravi{1}, Diego James{1}, Vineeth Sarma{1}, Bibhu Datta Sahoo{3}, Amol Inamdar{2}
{1}Amrita Vishwa Vidyapeetham University, India; {2}Hypres Inc., New York, United States; {3}University of Illinois at Urbana-Champaign, United States

Cryptography & PUF Circuits
Time: Tuesday, May 30 (11:00-12:30)
Room: Laurel AB
Chair(s): Maire O'Neill - Queens University; Weiqiang Liu - Nanjing University of Aeronautics and Astronautics

11:00 ***Fast Inversion in GF(2^m) with Polynomial Basis Using Optimal Addition Chains***
Lijuan Li, Shuguo Li
Tsinghua University, China

11:18 ***XOR Gate Based Low-Cost Configurable RO PUF***
Lei Zhang{1}, Chenghua Wang{1}, Weiqiang Liu{1}, Maire O'Neill{3}, Fabrizio Lombardi{2}
{1}Nanjing University of Aeronautics and Astronautics, China; {2}Northeastern University, United States; {3}Queen's University Belfast, United Kingdom

11:36 ***Investigation of DRAM PUFs Reliability Under Device Accelerated Aging Effects***
Fatemeh Tehranipoor, Nima Karimian, Wei Yan, John Chandy
University of Connecticut, United States

11:54 ***A Technique to Transform 6T-SRAM Arrays Into Robust Analog PUF with Minimal Overhead***
Jiangyi Li, Teng Yang, Mingoo Seok
Columbia University, United States

Networks-on-Chip
Time: Tuesday, May 30 (11:00-12:30)
Room: Laurel CD
Chair(s): Emre Salman - Stony Brook University; Shuenn-Yuh Lee - National Cheng Kung University

11:00 ***A Low Latency Fault Tolerant Transmission Mechanism for Network-on-Chip***
Letian Huang, Xinxin Lin, Junshi Wang, Qiang Li
University of Electronic Science and Technology of China, China

11:18 ***A Two-Stage Variation-Aware Task Mapping Scheme for Fault-Tolerant Multi-Core Network-on-Chips***
Lei Zhang{1}, Jianxun Yang{2}, Chengbo Xue{1}, Yue Ma{1}, Shan Cao{1}
{1}Beijing Institute of Technology, China; {2}Tsinghua University, China

11:36 ***Runtime Mitigation of Illegal Packet Request Attacks in Networks-on-Chip***
N Prasad, Rajit Karmakar, Santanu Chattopadhyay, Indrajit Chakrabarti
Indian Institute of Technology Kharagpur, India

11:54 ***Comprehensive Performance and Robustness Analysis of 2D Turn Models for Network-on-Chips***
Siavoosh Payandeh Azad{1}, Behrad Niazmand{1}, Karl Janson{1}, Thilo Kogge{3}, Jaan Raik{1}, Gert Jervan{1}, Thomas Hollstein{2}
{1}Tallinn University of Technology, Estonia; {2}Tallinn University of Technology / Frankfurt University of Applied Sciences, Germany; {3}Technische Universität Darmstadt, Germany

12:12 ***Implications of Noise Insertion Mechanisms of Different Countermeasures Against Side-Channel Attacks***
Weize Yu, Selcuk Köse
University of South Florida, United States

Multimedia Content Analysis & Retrieval
Time: Tuesday, May 30 (11:00-12:30)
Room: Kent AB
Chair(s): Yeong-Kang Lai - National Chung Hsing University; Shao-Yi Chien - National Taiwan University

11:00 ***Implicit Analysis of Perceptual Multimedia Experience Based on Physiological Response: a Review***
Seong-Eun Moon, Jong-Seok Lee
Yonsei University, Korea, South

11:18 ***A New Algorithm for Accurate and Automatic Chessboard Corner Detection***
Yuchi Zhang, Guolin Li, Xiang Xie, Zhihua Wang
Tsinghua University, China

11:36 ***Better Deep Visual Attention with Reinforcement Learning in Action Recognition***
Gang Wang{1}, Wenmin Wang{1}, Jingzhuo Wang{1}, Yaohua Bu{2}
{1}Peking University, China; {2}Tsinghua University, China

11:54 ***Cross-Domain Shoe Retrieval Using a Three-Level Deep Feature Representation***
Huijing Zhan{1}, Boxin Shi{2}, Alex Kot{1}
{1}Nanyang Technological University, Singapore; {2}National Institute of Advanced Industrial Science and Technology, Japan

12:12 ***A 120 fps 1080p Resolution Block-Based Feature Extraction Architecture Implementation for Real-Time Action Recognition***
Chun-Ting Yen, Wan-Yu Chen, Liang-Gee Chen
National Taiwan University, Taiwan

Video Interfaces & High Speed IO
Time: Tuesday, May 30 (11:00-12:30)
Room: Essex AB
Chair(s): Eduard Alarcon - Universitat Politècnica de Catalunya

11:00 ***A Real-Time FHD Learning-Based Super-Resolution System Without a Frame Buffer***
Kuan-Ling Liu, Ming-Che Yang, Shao-Yi Chien
National Taiwan University, Taiwan

11:18 ***A 55.1 mW 1.62-to-8.1 Gb/s Video Interface Receiver Generating Up to 680 MHz Stream Clock Over 20 dB Loss Channel***
Kwanseo Park, Jinhyung Lee, Kwangho Lee, Deog-Kyoon Jeong
Seoul National University, Korea, South

11:36 ***A 28-Gb/s 1.6-pJ/b PAM-4 Transmitter with 3-Tap FFE and Gm-Regulated Resistive-Feedback Inverter Based Drivers in 28-nm CMOS***
Haram Ju, Moon-Chul Choi, Deog-Kyoon Jeong
Seoul National University, Korea, South

11:54 ***A Frequency Reconfigurable 360° Analog Phase Shifter with a Constant Loss***
Fatemeh Akbar, Amir Mortazawi
University of Michigan, United States

12:12 ***A 4GS/s Reconfigurable Folding Flash ADC for Time Interleaving in 16nm FinFET***
Luke Wang{2}, Marcandre Lacroix{1}, Anthony Chan Carusone{2}
{1}Huawei Technologies Canada, Canada; {2}University of Toronto, Canada

Modeling & Analysis of Nonlinear Circuits
Time: Tuesday, May 30 (13:30-15:00)
Room: Dover A
Chair(s): Sergio Callegari - Università di Bologna; Elena Blokhina - University College Dublin

13:30 ***Closed-Form Model for Dual-Gate Ambipolar CNTFET Circuit Design***
Xuan Hu, Joseph Friedman
University of Texas at Dallas, United States

13:48 ***Variability of Supercapacitor Fractional-Order Parameters Extracted from Discharging Behavior Using Least Squares Optimization***
Todd Freeborn{1}, Ahmed Elwakil{2}
{1}University of Alabama, United States; {2}University of Sharjah, U.A.E.

14:06 ***Analysis of Power Consumption in LC Oscillators Based on the Inversion Coefficient***
Francesco Chicco, Alessandro Pezzotta, Christian Enz
École Polytechnique Fédérale de Lausanne, Switzerland

14:24 ***Coefficient Extraction for MPM Using LSE, ORLS and SLS Applied to RF-PA Modeling***
Jose Cruz Núñez Pérez{2}, Edgar Allende-Chávez{3}, Jose Ricardo Cárdenas-Valdez{3}, Esteban Tlelo-Cuautle{1}
{1}Instituto Nacional de Astrofísica, Óptica y Electrónica, Mexico; {2}Instituto Politecnico Nacional, Mexico; {3}Instituto Tecnologico de Tijuana, Mexico

14:42 ***Analysis and Comparison of Charge-Pump Conditioning Circuits for Capacitive Electromechanical Energy Conversion***
Armine Karami{1}, Dimitri Galayko{1}, Mohammed Bedier{1}, Philippe Basset{2}
{1}Laboratoire d'informatique de Paris 6 / Université Pierre et Marie Curie / Sorbonne Universités, France; {2}Université Paris-Est - ESIEE, France

Power Converters II
Time: Tuesday, May 30 (13:30-15:00)
Room: Dover BC
Chair(s): Hirotaka Koizumi - Tokyo University of Agriculture and Technology; Stefano Gregori - University of Guelph

13:30 ***Master-Slave Battery Charging System Using Parallel DC-DC Converters for Thermal Safety***
John Hu, Suming Lai
Maxim Integrated, United States

13:48 ***A Hybrid Nine-Level Inverter with Series/Parallel Conversion***
Yuya Nakagawa, Hirotaka Koizumi
Tokyo University of Science, Japan

14:06 ***A 0.9-V Input PWM DCM Boost Converter with Low Output Ripples and Fast Load Transient Response Based on a Novel Square-Root Voltage Mode (SRVM) Control Approach***
Hao Luo, Liter Siek
Nanyang Technological University, Singapore

14:24 ***A High-Speed Level Shifting Technique and its Application in High-Voltage, Synchronous DC-DC Converters with Quasi-ZVS***
Arunkumar Salimath{2}, Giovanni Gonano{1}, Edoardo Bonizzoni{2}, Davide Luigi Brambilla{1}, Edoardo Botti{1}, Franco Maloberti{2}
{1}STMicroelectronics, Italy; {2}Università degli Studi di Pavia, Italy

14:42 ***Design Trade-Offs of Integrated Polygonal Inductors for DC-DC Power Converters***
Ahmed Shaltout, Stefano Gregori
University of Guelph, Canada

Neural Arrays
Time: Tuesday, May 30 (13:30-15:00)
Room: Grand Ballroom I
Chair(s): Arindam Basu - Nanyang Technological University; Wei Xing Zheng - Western Sydney University

13:30 ***INVITED: Intelligent Virtual Agents at the Edge***
M. Anthony Lewis
Qualcomm Inc., United States

13:48 ***Dynamic Voltage and Frequency Scaling for Neuromorphic Many-Core Systems***
Sebastian Höppner{1}, Yexin Yan{1}, Bernhard Vogginger{1}, Andreas Dixius{1}, Johannes Partzsch{1}, Felix Neumärker{1}, Stephan Hartmann{1}, Stefan Schiefer{1}, Stefan Scholze{1}, Georg Ellguth{1}, Love Cederstroem{1}, Matthias Eberlein{1}, Christian Mayr{1}, Steve Temple {2}, Luis Plana{2}, Jim Garside{2}, Simon Davison{2}, David R. Lester{2}, Steve Furber{2}
{1}Technische Universität Dresden, Germany; {2}University of Manchester, United Kingdom

14:06 ***Scalable Bio-Inspired Fault Detection to Support Fault Recovery in Networks-on-Chip***
Malachy McElholm, Jim Harkin, Junxiu Liu, Liam McDaid
Ulster University, United Kingdom

14:24 ***A 65-nm CMOS 7fJ Per Synaptic Event Clique-Based Neural Network in Scalable Architecture***
Benoit Larras{2}, Paul Chollet{1}, Cyril Lahuec{1}, Fabrice Seguin{1}, Matthieu Arzel{1}
{1}TELECOM Bretagne, France; {2}Université Lille 1 / Université de Valenciennes, France

14:42 ***A Biological-Realtime Neuromorphic System in 28 nm CMOS Using Low-Leakage Switched Capacitor Circuits***
Christian Mayr, Johannes Partzsch, Marko Noack, Stefan Hänzsche, Stefan Scholze, Sebastian Höppner, Georg Ellguth, Rene Schüffny
Technische Universität Dresden, Germany

DSP for Biosignals
Time: Tuesday, May 30 (13:30-15:00)
Room: Grand Ballroom II
Chair(s): Keshab K. Parhi - University of Minnesota at Minneapolis; Peter Lian - York University

13:30 ***Pupil Localization for Gaze Estimation Using Unsupervised Graph-Based Model***
Salah Rabba{1}, Yifeng He{1}, Matthew Kyan{2}, Ling Guan{1}
{1}Ryerson University, Canada; {2}York University, Canada

13:48 ***Statistical Modeling of Multimodal Neuroimaging Data in Non-Subsampled Shearlet Domain Using the Student's t Location-Scale Distribution***
Emimal Jabason, M. Omair Ahmad, M.N.S. Swamy
Concordia University, Canada

14:06 ***Dynamic Gene Regulatory Network Analysis Using Saccharomyces cerevisiae Large-Scale Time-Course Microarray Data***
Li Zhang, Ho-Chun Wu, Jian-Qiang Lin, Shing-Chow Chan
University of Hong Kong, Hong Kong

14:24 ***Low-Power Real-Time ECG Baseline Wander Removal: Hardware Implementation***
Onur Guven{1}, Amir Eftekhar{1}, Wilko Kindt{2}, Timothy Constandinou{1}
{1}Imperial College London, United Kingdom; {2}Texas Instruments Inc., Netherlands

14:42 ***Constrained Kalman Filter for Improving Kinect Based Measurements***
Soumya Ranjan Tripathy{2}, Kingshuk Chakravarty{2}, Aniruddha Sinha{2}, Debatri Chatterjee{2}, Sanjoy Kumar Saha{1}
{1}Jadavpur University, India; {2}Tata Consultancy Services Ltd., India

RF Circuits II
Time: Tuesday, May 30 (13:30-15:00)
Room: Grand Ballroom III
Chair(s): Thierry Taris - Laboratoire de l'Intégration du Matériau au Système; Ioannis Syllaios - University of Texas at Dallas

13:30 ***Reconfigurable Inductorless Wideband CMOS LNA for Wireless Communications***
Thierry Taris{2}, Marcelo De Souza{1}, Andre Mariano{1}
{1}University Federal of Parana, Brazil; {2}University of Bordeaux, France

13:48 ***A Wideband RF Power Detector with -56 dB Sensitivity and 64 dB Dynamic Range in SiGe BiCMOS Technology***
Sreekesh Lakshminarayanan, Klaus Hofmann
Technische Universität Darmstadt, Germany

14:06 ***An 89 µW MICS/ISM Band Receiver for Ultra-Low-Power Applications***
Zexue Liu, Fan Yang, Haoyun Jiang, Xiucheng Hao, Junhua Liu, Huailin Liao
Peking University, China

14:24 ***A Transformer-Less Duplexer with Out-of-Band Filtering for Same-Channel Full-Duplex Radios***
Prateek Kumar Sharma, Nagarjuna Nallam
Indian Institute of Technology Guwahati, India

14:42 ***A Low Phase Noise 8.8 GHz VCO Based on ISF Manipulation and Dual-Tank Technique***
Rong Jiang{1}, Hossein Noori{1}, Fa Dai{1}, Jun Fu{2}, Wei Zhou{2}, Yudong Wang{2}
{1}Auburn University, United States; {2}Tsinghua University, China

PUF Circuits & Hardware Trojans
Time: Tuesday, May 30 (13:30-15:00)
Room: Grand Ballroom IV
Chair(s): Chip Hong Chang - Nanyang Technological University; Inna Partin Vaisband - University of Illinois at Chicago

13:30 ***An Entropy Test for Determining Whether a Mux PUF Is Linear or Nonlinear***
Anoop Koyily, Chen Zhou, Chris H. Kim, Keshab K. Parhi
University of Minnesota Twin Cities, United States

13:48 ***Low-Cost Fortification of Arbiter PUF Against Modeling Attack***
Siarhei S. Zalivaka{2}, Alexander A. Ivaniuk{1}, Chip-Hong Chang{2}
{1}Belarusian State University of Informatics and Radioelectronics, Belarus; {2}Nanyang Technological University, Singapore

14:06 ***Enhancing PUF Reliability by Machine Learning***
Yuejiang Wen, Yingjie Lao
Clemson University, United States; Clemson University , United States

14:24 ***Single-Triggered Hardware Trojan Identification Based on Gate-Level Circuit Structural Characteristics***
Fuqiang Chen, Qiang Liu
Tianjin University, China

14:42 ***HTChecker: Detecting Hardware Trojans Based on Static Characteristics***
Haihua Shen, Yuehui Zhao
University of the Chinese Academy of Sciences, China

Amplifiers & Analog Filtering
Time: Tuesday, May 30 (13:30-15:00)
Room: Grand Ballroom VII
Chair(s): Joseph Chang - Nanyang Technological University; Nuno Paulino - UNINOVA

13:30 ***Continuous Class-B/J Power Amplifier Using Nonlinear Embedding Technique: Analyzing the Design Space***
Samarth Saxena{1}, Karun Rawat{1}, Patrick Roblin{2}
{1}Indian Institute of Technology Roorkee, India; {2}Ohio State University, United States

13:48 ***Area-Efficient Fully Integrated Dual-Band Class-E/F Power Amplifier with Switchable Output Power for a BPSK/OOK Transmitter***
Christopher Soell{2}, Juergen Roeber{2}, Heinrich Milosiu{1}, Robert Weigel{2}, Amelie Hagelauer{2}
{1}Fraunhofer Institute for Integrated Circuits IIS, Germany; {2}Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany

14:06 ***A Multi-Path Ring Amplifier with Dynamic Biasing***
Jason Muhlestein{1}, Farshad Farahbakhshian{2}, Praveen Kumar Venkatachala{1}, Un-Ku Moon{1}
{1}Oregon State University, United States; {2}Texas Instruments Inc., United States

14:24 ***A Highly Compact Wideband Continuous-Time Transimpedance Low-Pass Filter***
Yang Xu, Praveen Kumar Venkatachala, Un-Ku Moon
Oregon State University, United States

14:42 ***Improved Nauta Transconductor for Wideband Intermediate-Frequency gm-C Filter***
Jianghui Deng{1}, Zhuojian Fu{1}, Zhao Wang{1}, Dihu Chen{1}, Xian Tang{2}, Jianping Guo{1}
{1}Sun Yat-sen University, China; {2}Tsinghua University, China

Flexible Internet of Things: From Devices to Systems
Time: Tuesday, May 30 (13:30-15:00)
Room: Grand Ballroom VIII
Chair(s): Xiaojun Guo - Shanghai Jiao Tong University; Yongpan Liu - Tsinghua University

13:30 ***Printed Organic TFT Sensor Tags***
Tse Nga Ng
University of California, San Diego, United States

13:48 ***Robust Design and Design Automation for Flexible Hybrid Electronics***
Tsung-Ching Huang{1}, Leilai Shao{4}, Ting Lei{3}, Ray Beausoleil{1}, Zhenan Bao{3}, Kwang-Ting Cheng{2}
{1}Hewlett Packard Labs, United States; {2}Hong Kong University of Science and Technology, China; {3}Stanford University, United States; {4}University of California, Santa Barbara, United States

14:06 ***An 8b 0.8kS/s Configurable VCO-Based ADC Using Oxide TFTs with Inkjet Printing Interconnection***
Wenyu Sun{3}, Qinghang Zhao{3}, Fei Qiao{3}, Yongpan Liu{3}, Huazhong Yang{3}, Xiaojun Guo{1}, Lei Zhou{2}, Lei Wang{2}
{1}Shanghai Jiao Tong University, China; {2}South China University of Technology, China; {3}Tsinghua University, China

Integrated Biomedical Systems, BioMEMS & Biosensors/Actuators I
Time: Tuesday, May 30 (13:30-15:00)
Room: Grand Ballroom IX
Chair(s): Mohamad Sawan - Polytechnique Montréal; Ibrahim Elfadel - Masdar Institute

13:30 ***A Stimulation Platform for Optogenetic and Bionic Vision Restoration***
Francesco Galluppi{2}, Didier Pruneau{2}, Joel Chavas{2}, Xavier Lagorce{1}, Christoph Posch{1}, Guillaume Chenegros{3}, Gilles Cordurié{3}, Charlie Galle{3}, Nicolas Oddo{3}, Ryad Benosman{3}
{1}Chronocam, France; {2}Gensight Biologics, France; {3}Université Pierre-et-Marie-Curie, France

13:48 ***A Miniaturized Low Power Biomedical Sensor Node for Clinical Research and Long Term Monitoring of Cardiovascular Signals***
Jarno Tuominen, Eero Lehtonen, Mojtaba Jafari Tadi, Juho Koskinen, Mikko Pänkäälä, Tero Koivisto
University of Turku, Finland

14:06 ***An Efficient Electronic Measurement Interface for Memristive Biosensors***
Sébastien Naus{2}, Ioulia Tzouvadaki{1}, Pierre-Emmanuel Gaillardon{3}, Armando Biscontini{3}, Giovanni De Micheli{1}, Sandro Carrara{1}
{1}École Polytechnique Fédérale de Lausanne, Switzerland; {2}Université de Liège, Belgium; {3}University of Utah, United States

14:24 ***Analyte Sampling in Paper Biosensors Powered by Graphite-Based Light Absorption***
Mingquan Yuan, Keng-Ku Liu, Srikanth Singamaneni, Shantanu Chakrabartty
Washington University in St. Louis, United States

14:42 ***An Implantable 128-Channel Wireless Neural-Sensing Microsystem Using TSV-Embedded Dissolvable μ-Needle Array and Flexible Interposer***
Po-Tsang Huang{3}, Yu-Chieh Huang{3}, Shang-Lin Wu{3}, Yu-Chen Hu Hu{3}, Ming-Wei Lu{3}, Ting-Wei Sheng{3}, Fung-Kai Chang{3}, Chun-Pin Lin{4}, Nien-Shang Chang{2}, Hung-Lieh Chen{2}, Chi-Shi Chen{2}, Jeng-Ren Duann{1}, Tzai-Wen Chiu{3}, Wei Hwang{3}, Kua-Neng Chen{3}, Ching-Te Chuang{3}, Jin-Chern Chiou{2}
{1}China Medical University, Taiwan; {2}Nation Chip Implementation Center, Taiwan; {3}National Chiao Tung University, Taiwan; {4}National Chip Implementation Center, Taiwan

Digital to Analog Conversion
Time: Tuesday, May 30 (13:30-15:00)
Room: Grand Ballroom X
Chair(s): Randall Geiger - Iowa State University; Tong Ge - Nanyang Technological University

13:30 ***A 14-Bit 2.5 Gs/s Digital Pre-Distorted DAC in 65 nm CMOS with SFDR > 70 dB Up to 1.2 GHz***
Zhiheng Zuo, Qingjun Fan, Jinghong Chen
University of Houston, United States

13:48 ***A Digital Calibration Technique Canceling Non-Linear Switch and Package Impedance Effects of a 1.6 GS/s TX-DAC in 28 nm CMOS***
Hossein Ghafarian, Friedel Gerfers
Technische Universität Berlin, Germany

14:06 ***A 13Bit 200MS/s Pipeline ADC with Current-Mode MDACs***
Carlos Briseno-Vidrios{1}, Dadian Zhou{2}, Suraj Prakash{2}, Qiyuan Liu{2}, Alexander Edward{2}, Jose Silva-Martinez{2}
{1}Silicon Labs, United States; {2}Texas A&M University, United States

14:24 ***The Analytic Expression of the Output Spectrum of ΔΣ ADCs with Nonlinear Binary-Weighted DACs and Gaussian Input Signals***
Ghyslain Gagnon{1}, François Gagnon{1}, Gordon Roberts{2}
{1}École de Technologie Supérieure, Canada; {2}McGill University, Canada

Communication & Timing Circuits
Time: Tuesday, May 30 (13:30-15:00)
Room: Laurel AB
Chair(s): Jin-Ku Kang - Inha University; Shoba Krishnan - Santa Clara University

13:30 ***A Low Latency and Area Efficient FFT Processor for Massive MIMO Systems***
Mojtaba Mahdavi, Ove Edfors, Viktor Öwall, Liang Liu
Lund University, Sweden

13:48 ***A 1 Gpps Asynchronous Logic OOK IR-UWB Transmitter Based on Master-Slave PLL Synthesis***
Marco Crepaldi, Gian Nicola Angotzi, Antonio Maviglia, Luca Berdondini
Istituto Italiano di Tecnologia, Italy

14:06 ***Settling Time of Mesochronous Clock Re-Timing Circuits in the Presence of Timing Jitter***
Naveen Kadayinti, Amitalok Budkuley, Dinesh Sharma
Indian Institute of Technology Bombay, India

14:24 ***Hardware Optimization of the Perturbation for Probabilistic Gradient Descent Bit Flipping Decoders***
Khoa Le{1}, Fakhreddine Ghaffari{1}, David Declercq{1}, Bane Vasic{2}
{1}École Nationale Supérieure de l'Électronique et de ses Applications, France; {2}University of Arizona, United States

14:42 ***25-Gb/s Clock and Data Recovery IC Using Latch-Load Combined with CML Buffer Circuit for Delay Generation with 65-nm CMOS***
Tomonori Tanaka{2}, Kosuke Furuichi{2}, Hiromu Uemura{2}, Ryousuke Noguchi{2}, Natsuyuki Koda{2}, Koki Arauchi{2}, Daichi Omoto{2}, Hiromi Inaba{2}, Keiji Kishine{2}, Shinsuke Nakano{1}, Masafumi Nogawa{1}, Hideyuki Nosaka{1}
{1}NTT Communications Corporation, Japan; {2}University of Shiga Prefecture, Japan

Memory Circuits
Time: Tuesday, May 30 (13:30-15:00)
Room: Laurel CD
Chair(s): Lan-Da Van - National Chiao Tung University; Yuan-Hao Huang - National Tsing Hua University

13:30 ***Area-Efficient STT/CMOS Non-Volatile Flip-Flop***
Jaeyoung Park
University of Texas at Austin, United States

13:48 ***TCache: an Energy-Efficient DRAM Cache Design***
Jiacong He, Joseph Callenes-Sloan
University of Texas at Dallas, United States

14:06 ***Effective Write-Reduction Method for MLC Non-Volatile Memory***
Masashi Tawada, Shinji Kimura, Masao Yanagisawa, Nozomu Togawa
Waseda University, Japan

14:24 ***A New Write-Contention Based Dual-Port SRAM PUF with Multiple Response Bits Per Cell***
Chao Qun Liu, Yue Zheng, Chip-Hong Chang
Nanyang Technological University, Singapore

Video Coding & Multimedia System Architecture
Time: Tuesday, May 30 (13:30-15:00)
Room: Kent AB
Chair(s): Chris Lee - National Cheng Kung University; Shao-Yi Chien - National Taiwan University

13:30 ***A Fast Intra Encoding Platform for AVS2***
Kui Fan, Ronggang Wang, Zhenyu Wang, Ge Li, Wen Gao
Peking University, China

13:48 ***High-Throughput HEVC Intrapicture Prediction Hardware Design Targeting UHD 8K Videos***
Marcel Corrêa, Bruno Zatt, Marcelo Porto, Luciano Agostini
Universidade Federal de Pelotas, Brazi

14:06 ***VLSI Architecture Design of Layer-Based Bilateral and Median Filtering for 4k2k Videos at 30fps***
Ming-Yi Tai, Wei-Chih Tu, Shao-Yi Chien
National Taiwan University, Taiwan

14:24 ***A Multiplierless Parallel HEVC Quantization Hardware for Real-Time UHD 8K Video Coding***
Luciano Braatz, Luciano Agostini, Bruno Zatt, Marcelo Porto
Universidade Federal de Pelotas, Brazil

14:42 ***Corner Proposals from HEVC Bitstreams***
Hyomin Choi, Ivan Bajić
Simon Fraser University, Canada

Applied Signal Processing & Deep Learning
Time: Tuesday, May 30 (13:30-15:00)
Room: Essex AB
Chair(s): Eduard Alarcon - Universitat Politècnica de Catalunya

13:30 ***Fully-Parallel Area-Efficient Deep Neural Network Design Using Stochastic Computing***
Yi Xie{1}, Siyu Liao{1}, Bo Yuan{1}, Yanzhi Wang{3}, Zhongfeng Wang{2}
{1}City University of New York, United States; {2}Nanjing University, United States; {3}Syracuse University, United States

13:48 ***Bringing Offline Mining to Online Learning System: Low-Cost and Efficient Self-Healing Synaptic Storage for Deep Learning***
Jonathon Edstrom, Dongliang Chen, Yifu Gong, Jinhui Wang, Na Gong
North Dakota State University, United States

14:06 ***Deep Texture Features for Robust Face Spoofing Detection***
Gustavo Souza{2}, Daniel Santos{1}, Rafael Pires{2}, Aparecido Marana{1}, João Papa{1}
{1}São Paulo State University, Brazil; {2}Universidade Federal de São Carlos, Brazil

14:24 ***Chattering Free Fixed-Time Convergent Sliding Mode Controller***
Jyoti Prakash Mishra, Xinghuo Yu, Mahdi Jalili
Royal Melbourne Institute of Technology, Australia

14:42 ***Accurate Spectral Testing with Non-Coherent Sampling for Multi Tone Applications***
Yuming Zhuang, Degang Chen
Iowa State University, United States

LIVE DEMONSTRATIONS – TUESDAY, MAY 30TH

Demonstration Session II
Time: Tuesday, May 30 (13:30-16:30)
Room: Harborside Ballroom
Chair(s): Jennifer Blain Christen - Arizona State University; Shih-Chii Liu - Swiss Federal Institute of Technology in Zurich

O-1 - Live Demonstration: Automated Data Acquisition and Digital Curation Platform for Enhancing Research Precision, Productivity and Reproducibility
Yousef Gtat, Sina Parsnejad, Andrew J. Mason
Michigan State University, United States

O-2 - Live Demonstration: Unipolar Symmetrical Variable-Capacitance Generators for Energy Harvesting
Antonio de Queiroz, Luiz de Oliveira Filho
Universidade Federal do Rio de Janeiro, Brazil

O-3 - Live Demonstration: a Wearable EIT System Using Active Electrodes for Monitoring Respiration
Yu Wu{2}, Dai Jiang{2}, Andy Bardill{1}, Serena De Gelidi{1}, Richard Bayford{1}, Andreas Demosthenous{2}
{1}Middlesex University, United Kingdom; {2}University College London, United Kingdom

O-4 - Live Demo of a Vibration-Powered Bluetooth Sensor with Running PFC Power Conditioning
Kang Zhao, Yuheng Zhao, Junrui Liang
ShanghaiTech University, China

O-5 - Live Demonstration: Depth from Focus on a Focal Plane Processor Using a Focus Tunable Liquid Lens
Julien N.P. Martel{1}, Lorenz K. Müller{1}, Stephen J. Carey{2}, Jonathan Müller{1}, Yulia Sandamirskaya{1}, Piotr Dudek{2}
{1}Universität Zürich / Eidgenössische Technische Hochschule Zürich, Switzerland; {2}University of Manchester, United Kingdom

O-6 - Live Demonstration: a Wirelessly Powered Highly Miniaturized Neural Stimulator
Adam Khalifa{1}, Sherry Chiu{1}, Yasha Karimi{2}, Milutin Stanaćević{2}, Ralph Etienne-Cummings{1}
{1}Johns Hopkins University, United States; {2}Stony Brook University, United States

O-7 - Live Demonstration: Behaving Cyborg Locusts for Standoff Chemical Sensing
Darshit Mehta, Ege Altan, Rishabh Chandak, Baranidharan Raman, Shantanu Chakrabartty
Washington University in St. Louis, United States

O-8 - Live Demonstration: Prosthesis Grip Force Modulation Using Neuromorphic Tactile Sensing

Luke Osborn{2}, Harrison Nguyen{2}, Rahul Kaliki{1}, Nitish Thakor{3}
{1}Infinite Biomedical Technologies, United States; {2}Johns Hopkins University, United States; {3}Johns Hopkins University / National University of Singapore, United States

O-9 - Live Demonstration - an Adaptable Prosthetic Socket: Regulating Independent Air Bladders Through Closed-Loop Control

Daniel Candrea{1}, Avinash Sharma{3}, Luke Osborn{4}, Yikun Gu{2}, Nitish Thakor{5}
{1}Duke University, United States; {2}Harbin Institute of Technology, China; {3}Indian Institute of Technology Delhi, India; {4}Johns Hopkins University, United States; {5}Johns Hopkins University / National University of Singapore, United States

O-10 - Live Demonstration: Real-Time, Dynamic Visual Saliency Computation in a VR Environment Seeing Through the Eyes of a Mobile Robot

Jamal Molin{1}, Christopher Simmons{1}, Garrett Nixon{2}, Ralph Etienne-Cummings{1}
{1}Johns Hopkins University, United States; {2}Sidwell Friends High School, United States

O-11 - Live Demonstration: a CMOS-Based ISFET Array for Rapid Diagnosis of the Zika Virus

Nicolas Moser, Jesus Rodriguez-Manzano, Ling-Shan Yu, Melpomeni Kalofonou, Sara de Mateo, Xiaoxiang Li, Tor Sverre Lande, Christofer Toumazou, Pantelis Georgiou
Imperial College London, United Kingdom

O-12 - Live Demonstration: Real-Time Chemical Imaging of Ionic Solutions Using an ISFET Array

Nicolas Moser, Chi Leng Leong, Yuanqi Hu, Martyn Boutelle, Pantelis Georgiou
Imperial College London, United Kingdom

O-13 - Live Demonstration: a Highly Sensitive and Quantitative Fluorescence Sensing Platform, for Disease Diagnosis

Uwadiae Obahiagbon, Joseph Smith, Hany Arafa, Dixie Kullman, Jennifer Blain Christen
Arizona State University, United States

O-14 - Live Demonstration: a Wireless Headstage Enabling Combined Optogenetics and Multichannel Electrophysiological Recording

Gabriel Gagnon-Turcotte{2}, Yoan Lechasseur{1}, Cyril Bories{2}, Younès Messaddeq{2}, Yves De Koninck{2}, Benoit Gosselin{2}
{1}Doric Lenses, Canada; {2}Université Laval, Canada

O-15 - Live Demonstration: a Multimodal Adaptive Wireless Control Interface for People with Upper-Body Disabilities

Cheikh Latyr Fall{2}, Francis Quevillon{2}, Alexandre Campeau-Lecours{2}, Simon Latour{1}, Martine Blouin{1}, Clément Gosselin{2}, Benoit Gosselin{2}
{1}Kinova Robotics, Canada; {2}Université Laval, Canada

O-16 - Live Demonstration: a Frequency-Based System for Wireless Electrical Stimulation of iEAPs

Yi Huang, Daniel Browe, Joseph Freeman, Laleh Najafizadeh
Rutgers University, United States

POSTER SESSION – TUESDAY, MAY 30TH

Integrated Biomedical Systems & BioMEMS
Time: Tuesday, May 30 (15:00-16:30)
Room: Harborside Ballroom
Chair(s): Nitish Thakor - Johns Hopkins University; Pantelis Georgiou - Imperial College London

O-17 - An Adaptable Prosthetic Socket: Regulating Independent Air Bladders Through Closed-Loop Control
Daniel Candrea{1}, Avinash Sharma{3}, Luke Osborn{4}, Yikun Gu{2}, Nitish Thakor{5}
{1}Duke University, United States; {2}Harbin Institute of Technology, China; {3}Indian Institute of Technology Delhi, India; {4}Johns Hopkins University, United States; {5}Johns Hopkins University / National University of Singapore, United States

O-18 - A Dual Switched-Capacitor Integrator Architecture for Versatile, Real-Time Amperometric Biosensing
Michail Pligouroudis, Konstantinos Papadimitriou, Daniel Evans, Themistoklis Prodromakis
University of Southampton, United Kingdom

O-19 - Iontophoresis Instrumentation for the Enhancement of Gene Therapy in Wound Healing
Martina Leistner{1}, Samantha Wang{1}, Ralph Etienne-Cummings{1}, Frank Lay{2}, Louis Born{2}, Zahra Alikhassy{2}, Ali Karim Ahmed{2}, John W. Harmon{2}
{1}Johns Hopkins University, United States; {2}Johns Hopkins University School of Medicine, United States

O-20 - pH Sensing Threads with CMOS Readout for Smart Bandages
Meera Punjiya{2}, Hojatollah Rezaei Nejad{2}, Pooria Mostafalu{1}, Sameer Sonkusale{2}
{1}Harvard University, United States; {2}Tufts University, United States

O-21 - A Multimodal Adaptive Wireless Control Interface for People with Upper-Body Disabilities
Cheikh Latyr Fall{2}, Francis Quevillon{2}, Alexandre Campeau-Lecours{2}, Simon Latour{1}, Martine Blouin{1}, Clément Gosselin{2}, Benoit Gosselin{2}
{1}Kinova Robotics, Canada; {2}Université Laval, Canada

O-22 - Dielectric Analysis of Changes in Electric Properties of Leukemic Cells Through Travelling and Negative Dielectrophoresis with 2-D Electrodes
Sameh Sherif{1}, Yehya H. Ghallab{2}, Hamdy Abd El Hamid{2}, Yehea Ismail{2}
{1}American University in Cairo, Egypt; {2}American University in Cairo / Zewail City of Science and Technology, Egypt

O-23 - Separation and Electrochemical Detection Platform for Portable Individual PM2.5 Monitoring
Heyu Yin, Hao Wan, Andrew J. Mason
Michigan State University, United States

O-24 - A 32-by-32 CMOS Microelectrode Array for Capacitive Biosensing and Impedance Spectroscopy
Virgilio Valente, Andreas Demosthenous
University College London, United Kingdom

O-25 - Characterization of a High Dynamic Range Lab-on-CMOS Capacitance Sensor Array
Bathiya Senevirathna, Sheung Lu, Pamela Abshire
University of Maryland, College Park, United States

Other Areas in Analog & Mixed Signal Circuits & Systems
Time: Tuesday, May 30 (15:00-16:30)
Room: Harborside Ballroom
Chair(s): Tong Ge - Nanyang Technological University; Igor Filanvosky - University of Alberta

P-26 - A New 1.8V Pierce-Gate Crystal Oscillator Based on the Constant gm Cell in 28nm CMOS Technology for Automotive Radar Applications
Giuseppe Macera, Patrick Crowley
Analog Devices Inc., Ireland

P-27 - A Merged Window Comparator Based Relaxation Oscillator with Low Temperature Coefficient
Lin Ma, Kuan Chuang Koay, Pak Kwong Chan
Nanyang Technological University, Singapore

P-28 - Multi-Band Inductor-Less VCO for IoT Applications
Fayrouz Haddad, Imen Ghorbel, Wenceslas Rahajandraibe
Universités de Toulon Laboratoire Materiaux et Microelectronique de Provence, France

P-29 - A 0.13 µm CMOS Fully Integrated 0.1~12 GHz Frequency Synthesizer for Avionic SDR Applications
Zakaria El Alaoui Ismaili{1}, Wessam Ajib{2}, François Gagnon{1}, Frédéric Nabki{1}
{1}École de Technologie Supérieure, Canada; {2}Université du Québec à Montréal, Canada

P-30 - A Charge Limiting and Redistribution Method for Delay Line Locking in Multi-Output Clock Generation
Yury Antonov, Kari Stadius, Jussi Ryynänen
Aalto University, Finland

P-31 - A 7μA 1.6ppm/°C Bandgap Design Realizable in CMOS Process
Kin Keung Jeff Lau
Silicon Mitus Technology, United States

P-32 - A PVT Resistant Coarse-Fine Time-to-Digital Converter
Esrafil Jedari, Rashid Rashidzadeh, Mehrdad Saif
University of Windsor, Canada

P-33 - A 0.6V 50-to-145MHz PVT Tolerant Digital PLL with DCO-Dedicated ΔΣ LDO and Temperature Compensation Circuits in 65nm CMOS
Yudong Zhang{1}, Xiaofeng Liu{2}, Woogeun Rhee{2}, Hanjun Jiang{2}, Zhihua Wang{2}
{1}Columbia University, United States; {2}Tsinghua University, China

P-34 - A Low-Power Temperature-Compensated CMOS Peaking Current Reference in Subthreshold Region
Mohammad Sadegh Eslampanah{1}, Siavash Kananian{4}, Elaheh Zendehrouh{5}, Mohammad Sharifkhani{3}, Amir Masoud Sodagar{2}, Mahdi Shabany{3}
{1}Georgia Institute of Technology, United States; {2}Khajeh Nasir Toosi University of Technology, Iran; {3}Sharif University of Technology, Iran; {4}Stanford University, United States; {5}West Tehran Islamic Azad University, Iran

P-35 - Analog Layout Density Uniformity Improvement Using Interconnect Widening and Dummy Fill Insertion
Gholamreza Shomalnasab{1}, Lihong Zhang{2}
{1}Memorial University, Canada; {2}Memorial University of Newfoundland, Canada

P-36 - A 5mW Batteryless Start-Up Boost Charger for Wireless Power Transfer
Seok-Tae Koh{1}, Se-Un Shin{1}, Yu-Jin Yang{1}, Minseong Choi{1}, Seungchul Jung{2}, Gyu-Hyung Cho{1}
{1}Korea Advanced Institute of Science and Technology, Korea, South; {2}Samsung Electronics, Korea, South

P-37 - Ultra Miniature Offset Cancelled Bandgap Reference with ±0. 534% Inaccuracy from -10°C to 110°C
Natan Vinshtok-Melnik, Robert Giterman, Joseph Shor
Bar-Ilan University, Israel

P-38 - Using Dynamic Dependence Analysis to Improve the Quality of High-Level Synthesis Designs
Rafael Garibotti, Brandon Reagen, Yakun Sophia Shao, Gu-Yeon Wei, David Brooks
Harvard University, United States

P-39 - DPA-Resistant QDI Dual-Rail AES S-Box Based on Power-Balanced Weak-Conditioned Half-Buffer
James Lim, Weng-Geng Ho, Kwen-Siong Chong, Bah-Hwee Gwee
Nanyang Technological University, Singapore

P-40 - A Voltage Reference Generator Targeted at Extracting the Silicon Bandgap VGO from VBE
Zhiqiang Liu, Degang Chen
Iowa State University, United States

P-41 - A Calibration-Free Low-Power Supply-Pushing Reduction Circuit (SPRC) for LC VCOs
Muhammad Ahmed Swilam, Ahmed Naguib, Brian Dupaix, Waleed Khalil, Ayman Fayed
Ohio State University, United States

P-42 - Deep Modeling: Circuit Characterization Using Theory Based Models in a Data Driven Framework
David Bolme{1}, Aravind Mikkilineni{1}, Derek Rose{1}, Srikanth Yoginath{1}, Mohsen Judy{2}, Jeremy Holleman{2}
{1}Oak Ridge National Laboratory, United States; {2}University of Tennessee, United States

P-43 - A Size-Adaptive Time-Step Algorithm for Accurate Simulation of Aging in Analog ICs
Pablo Martín-Lloret{1}, Antonio Toro-Frías{1}, Javier Martin-Martinez{2}, Rafael Castro-Lopez{1}, Elisenda Roca{1}, Rosana Rodríguez Martínez{2}, Montserrat Nafria{2}, Francisco V. Fernandez{1}
{1}Consejo Superior de Investigaciones Científicas / Universidad de Sevilla, Spain; {2}Universitat Autònoma de Barcelona, Spain

P-44 - Timing Speculative SRAM
Elnaz Ebrahimi, Matthew Guthaus, Jose Renau
University of California, Santa Cruz, United States

P-45 - Low Power Speech Detector on a FPAA
Sahil Shah, Jennifer Hasler
Georgia Institute of Technology, United States

P-46 - Wafer-Level Adaptive Trim Seed Forecasting Based on E-Tests
Constantinos Xanthopoulos{2}, Ali Ahmadi{2}, Sirish Boddikurapati{1}, Amit Nahar{1}, Bob Orr{1}, Yiorgos Makris{2}
{1}Texas Instruments Inc., United States; {2}University of Texas at Dallas, United States

P-47 - CMOS Current-Mode PWL Implementation Using MAX and MIN Operators
Oscar Jair Cinco-Izquierdo{1}, María Teresa Sanz-Pascual{1}, Luis Hernández{1}, Carlos Arostóteles de la Cruz-Blas{2}
{1}Instituto Nacional de Astrofísica, Óptica y Electrónica, Mexico; {2}Universidad Pública de Navarra, Spain

P-48 - An Efficient and Fair Scheduling Policy for Multiprocessor Platforms
Theodoros Marinakis{2}, Alexandros-Herodotos Haritatos{1}, Konstantinos Nikas{1}, Georgios Goumas{1}, Iraklis Anagnostopoulos{2}
{1}National Technical University Of Athens, Greece; {2}Southern Illinois University Carbondale, United States

P-49 - Design Methodology for Area and Energy Efficient OxRAM-Based Non-Volatile Flip-Flop
Mahesh Nataraj{4}, Alexandre Levisse{2}, Bastien Giraud{2}, Jean-Philippe Noel{2}, Pascal Meinerzhagen{3}, Jean-Michel Portal{1}, Pierre-Emmanuel Gaillardon{4}
{1}Aix-Marseille Universite, France; {2}Commissariat à l'Energie Atomique et aux Energies Alternatives, France; {3}Intel Research Lablets, United States; {4}University of Utah, United States

P-50 - An Analog Phase Prediction Based Fractional-N PLL
Aaron Bluestone, Ryan Kaveh, Luke Theogarajan
University of California, Santa Barbara, United States

DSP : Algorithms and Implementations
Time: Tuesday, May 30 (15:00-16:30)
Room: Harborside Ballroom
Chair(s): Arjuna Madanayake - University of Akron; Mohsin Jamali - University of Toledo

Q-51 - Pipeline Tracking and Event Classification for an Automatic Inspection Vision System
Felipe Petraglia, Roberto Campos, José Gabriel Gomes, Mariane Petraglia
Universidade Federal do Rio de Janeiro, Brazil

Q-52 - Fast Human-Animal Detection from Highly Cluttered Camera-Trap Images Using Joint Background Modeling and Deep Learning Classification
Hayder Yousif{2}, Jianhe Yuan{2}, Roland Kays{1}, Zhihai He{2}
{1}North Carolina State University, United States; {2}University of Missouri, United States

Q-53 - Face Hallucination Using Deep Collaborative Representation for Local and Non-Local Patches
Tao Lu{2}, Lanlan Pan{2}, Hao Wang{2}, Yanduo Zhang{2}, Bo Wang{1}, Zixiang Xiong{1}
{1}Texas A&M University, United States; {2}Wuhan Institute of Technology, China

Q-54 - A 0.53mW Ultra-Low-Power 3D Face Frontalization Processor for Face Recognition with Human-Level Accuracy in Wearable Devices
Sanghoon Kang, Jinmook Lee, Kyeongryeol Bong, Changhyeon Kim, Hoi-Jun Yoo
Korea Advanced Institute of Science and Technology, Korea, South

Q-55 - Single Image Super-Resolution Using Hybrid Patch Search and Local Self-Similarity
Shen-Li Lo, Ching-Te Chiu
National Tsing Hua University, Taiwan

Q-56 - Design of Composite Filters with Equiripple Passbands and Least-Squares Stopbands
Wu-Sheng Lu{2}, Takao Hinamoto{1}
{1}Hiroshima University, Japan; {2}University of Victoria, Canada

Q-57 - An Indirect Approach to Synthesis of Noise Shaping IIR Filters in ΔΣ Modulators
Muhammad Rizwan Tariq, Shuichi Ohno
Hiroshima University, Japan

Q-58 - Speech Recognition Using TVLPC Based MFCC for Similar Pronunciation Phrases
George Mufungulwa{1}, Alia Asheralieva{1}, Hiroshi Tsutsui{1}, Shini-Ichi Abe{2}, Yoshikazu Miyanaga{1}
{1}Hokkaido University, Japan; {2}Vehicle Information and Communication System Center, Japan

Q-59 - sWMF: Separable Weighted Median Filter for Efficient Large-Disparity Stereo Matching
Shiqiang Chen, Xuchong Zhang, Hongbin Sun, Nanning Zheng
Xi'an Jiaotong University, China

Q-60 - Joint-Domain Unsupervised Stylization for Portraits
Saboya Yang, Jiaying Liu, Shuai Yang, Wenhan Yang, Zongming Guo
Peking University, China

Q-61 - Census Transform-Based Static Caption Detection for Frame Rate Up-Conversion
Gyujin Bae{1}, Young Hwan Kim{1}, Suk-Ju Kang{2}
{1}Pohang University of Science and Technology, Korea, South; {2}Sogang University, Korea, South

Q-62 - Variable Pixel G-Neighbor Filters
Yerbol Akhmetov{2}, Joshin John Mathew{1}, Alex James{2}
{1}ARS Traffic & Transport Technology, India; {2}Nazarbayev University, Russia

Q-63 - FPGA Acceleration of Hyperspectral Image Processing for High-Speed Detection Applications
Simon Vellas, George Lentaris, Konstantinos Maragos, Dimitrios Soudris, Zacharias Kandylakis, Konstantinos Karantzalos
National Technical University of Athens, Greece

Q-64 - Throughput Evaluation of DSP Applications Based on Hierarchical Dataflow Model
Hamza Deroui{1}, Karol Desnos{1}, Jean-François Nezan{1}, Alix Munier-Kordon{2}
{1}Institut National des Sciences Appliquées de Rennes, France; {2}Laboratoire d'informatique de Paris 6 / Université Pierre et Marie Curie / Sorbonne Universités, France

Q-65 - Robust Speaker Verification with a Two Classifier Format and Feature Enhancement
Joshua Edwards, Ravi Ramachandran, Umashanger Thayasivam
Rowan University, United States

Q-66 - Sparse FIR Filter Design via Partial L1 Optimization
Li Zheng{1}, Aimin Jiang{1}, Hon Keung Kwan{2}
{1}Hohai University, China; {2}University of Windsor, Canada

Q-67 - A QCQP Design Method of the Symmetric Pulse-Shaping Filters Against Receiver Timing Jitter
Chia-Yu Yao, Shui-Chin Wang
National Taiwan University of Science and Technology, Taiwan

Q-68 - Least-Squares Estimation of the Common Acoustical Poles in Room Acoustics and Head Related Transfer Functions
Sahar Hashemgeloogerdi, Mark Bocko
University of Rochester, United States

Q-69 - Efficient Implementation of Modular Multiplication by Constants Applied to RNS Reverse Converters
Roberto de Matos{1}, Rogerio Paludo{3}, Nikolay Chervyakov{2}, Pavel Lyakhov{2}, Hector Pettenghi{3}
{1}Instituto Federal de Santa Catarina, Brazil; {2}North Caucasus Federal University, Russia; {3}Universidade Federal de Santa Catarina, Brazil

Q-70 - A New Electric Encoder Position Estimator Based on the Chinese Remainder Theorem for the CMG Performance Improvements
Gian Carlo Cardarilli{2}, Luca Di Nunzio{2}, Rocco Fazzolari{2}, Luca Gerardi{2}, Marco Re{2}, Giovanni Campolo{1}, Domenico Cascone{1}
{1}Thales Alenia Space, Italy; {2}Università degli Studi di Roma Tor Vergata, Italy

Nanoelectonics & Memristor Technology
Time: Tuesday, May 30 (15:00-16:30)
Room: Harborside Ballroom
Chair(s): Danella Zhao - University of Louisiana at Lafayette; Hao Jiang - San Francisco State University

R-71 - Exploring Logic Architectures Suitable for TFETs Devices
Juan Núñez, María J. Avedillo
Consejo Superior de Investigaciones Científicas / Universidad de Sevilla, Spain

R-72 - A High Performance Full Adder Based on Ballistic Deflection Transistor Technology
Poorna Marthi{2}, Nazir Hossain{2}, Huan Wang{2}, Jean-Francois Millithaler{2}, Martin Margala{2}, Ignacio Iñiguez-de-la-Torre{1}, Javier Mateos{1}, Tomas González{1}
{1}Universidad de Salamanca, Spain; {2}University of Massachusetts Lowell, United States

R-73 - A Compliance Current Circuit with Nanosecond Response Time for ReRAM Characterization
Qingjiang Li, Jinling Xing, Zhaolin Sun, Fei Jing, Hui Xu
National University of Defense Technology, China

R-74 - Transient Response Enhancement of RF MEMS Tuners Using Digital Signal Processing
Mohammad Abu Khater, Mahmoud Abdelfattah, Yu-Chiao Wu, Wesley Allen, Dimitrios Peroulis
Purdue University, United States

R-75 - A Unified Analytical Reliability Model of NBTI and HCD for Undoped Double Gate PMOS
Omnia Samy{1}, Hamdy Abd El Hamid{2}, Yehea Ismail{2}, Abd El Halim Zekry{3}
{1}Ain Shams University, Egypt; {2}American University in Cairo / Zewail City of Science and Technology, Egypt; {3}Arizona State University, Egypt

R-76 - Adapting Large-Area Flexible Hybrid TFT/CMOS Electronics and Display Technology to Create an Optical Sensor Array Architecture
Joseph Smith, Edward Bawolek, Jovan Trujillo, Gregory Raupp, David Allee, Jennifer Blain Christen
Arizona State University, United States

R-77 - Size-Dependent Switching Coherence of Elliptical Single-Domain Magnetostrictive Nanomagnets in Straintronic Circuit
Huanqing Cui, Li Cai, Li Xu, Sen Wang, Xiaokuo Yang, Chaowen Feng
Air Force Engineering University, China

R-78 - Process Variation Immune and Energy Aware Sense Amplifiers for Resistive Non-Volatile Memories
Soheil Salehi, Ronald F. DeMara
University of Central Florida, United States

R-79 - A TiO2 ReRAM Parameter Extraction Method
Ioannis Messaris{1}, Spyridon Nikolaidis{1}, Alexantrou Serb{2}, Spyros Stathopoulos{2}, Isha Gupta{2}, Ali Khiat{2}, Themistoklis Prodromakis{2}
{1}Aristotle University of Thessaloniki, Greece; {2}University of Southampton, United Kingdom

R-80 - A Practical Hafnium-Oxide Memristor Model Suitable for Circuit Design and Simulation
Sherif Amer{2}, Sagarvarma Sayyaparaju{2}, Garrett S. Rose{2}, Karsten Beckmann{1}, Nathaniel C. Cady{1}
{1}State University of New York Polytechnic Institute, United States; {2}University of Tennessee, United States

R-81 - Novel Hafnium Oxide Memristor Device: Switching Behaviour and Size Effect
Heba Abunahla, Baker Mohammad, Maguy Abi Jaoude, Mahmoud Al-Qutayri
Khalifa University, U.A.E.

R-82 - Design and Optimization of a Strong PUF Exploiting Sneak Paths in Resistive Cross-Point Array
Rui Liu, Pai-Yu Chen, Shimeng Yu
Arizona State University, United States

R-83 - A Pulse-Based Memristor Programming Circuit
Olufemi Akindele Olumodeji, Massimo Gottardi
Fondazione Bruno Kessler, Italy

R-84 - Test Point Insertion for RSFQ Circuits
Gleb Krylov, Eby G. Friedman
University of Rochester, United States

R-85 - A Memristor Based Image Sensor Exploiting Compressive Measurement for Low-Power Video Streaming
Fengyu Qian, Yanping Gong, Lei Wang
University of Connecticut, United States

R-86 - A Placement Management Circuit for Efficient Realtime Hardware Reuse on FPGAs Targeting Reliable Autonomous Systems
Godwin Enemali, Adewale Adetomi, Tughrul Arslan
University of Edinburgh, United Kingdom

Spiking and Learning Systems
Time: Tuesday, May 30 (15:00-16:30)
Room: Harborside Ballroom
Chair(s): Ricardo Carmona Galán - Instituto of Microelectrónica of Sevilla; Shoushun Chen - Nanyang Technological University

S-87 - PredictiveNet: an Energy-Efficient Convolutional Neural Network via Zero Prediction
Yingyan Lin, Charbel Sakr, Yongjune Kim, Naresh Shanbhag
University of Illinois at Urbana-Champaign, United States

S-88 - A Real-Time 17-Scale Object Detection Accelerator with Adaptive 2000-Stage Classification in 65nm CMOS
Minkyu Kim{1}, Abinash Mohanty{1}, Deepak Kadetotad{1}, Naveen Suda{2}, Luning Wei{3}, Pooja Saseendran{1}, Xiaofei He{3}, Yu Cao{1}, Jae-Sun Seo{1}
{1}Arizona State University, United States; {2}ARM, Inc., United States; {3}Zhejiang University, China

S-89 - Comparison of Three FPGA Architectures for Embedded Multidimensional Categorization Through Kohonen's Self-Organizing Maps
Miguel Sousa, Emilio Del-Moral-Hernandez
Universidade de São Paulo, Brazil

S-90 - Energy-Efficient Scheduling Method with Cross-Loop Model for Resource-Limited CNN Accelerator Designs
Kaiyi Yang, Shihao Wang, Jianbin Zhou, Takeshi Yoshimura
Waseda University , Japan; Waseda University, Japan

S-91 - Robust Reconstruction of Network Topology via Huber Algorithm
Juan Liu{1}, Jinhu Lü{1}, Maciej J. Ogorzalek{2}, Kexin Liu{3}
{1}Academy of Mathematics and Systems Science, Chinese Academy of Sciences, China; {2}Jagiellonian University, Poland; {3}Peking University, China

S-92 - Multiplexing AER Asynchronous Channels Over LVDS Links with Flow-Control and Clock-Correction for Scalable Neuromorphic Systems
Amirreza Yousefzadeh{2}, Miroslav Jabłoński{1}, Taras Iakymchuk{4}, Alejandro Linares-Barranco{3}, Alfredo Rosado{4}, Luis Plana{5}, Teresa Serrano-Gotarredona{2}, Steve Furber{5}, Bernabe Linares-Barranco{2}
{1}AGH University of Science and Technology, Poland; {2}Consejo Superior de Investigaciones Científicas / Universidad de Sevilla, Spain; {3}Universidad de Sevilla, Spain; {4}Universitat de València, Spain; {5}University of Manchester, United Kingdom

S-93 - Online Multiclass Passive-Aggressive Learning on a Fixed Budget
Chung-Hao Wu, Wei-Chen Hsi, Henry Horng-Shing Lu, Hsueh-Ming Hang
National Chiao Tung University, Taiwan

S-94 - Compact Digital-Controlled Neuromorphic Circuit with Low Power Consumption
Jin Zhang, Yuan Wang, Xing Zhang, Ru Huang
Peking University, China

S-95 - Neural Network Based ECG Anomaly Detection on FPGA and Trade-Off Analysis
Matthias Wess, Sai Dinakarrao, Axel Jantsch
Technische Universität Wien, Austria

S-96 - A Switched-Capacitor Dendritic Arbor for Low-Power Neuromorphic Applications
Pezhman Mamdouh, Alice Parker
University of Southern California, United States

S-97 - Taking Advantage of Correlation in Stochastic Computing
Rahul Kumar Budhwani{1}, Rengarajan Ragavan{2}, Olivier Sentieys{1}
{1}IRISA/ INRIA, University of Rennes, France; {2}University of Rennes, France

S-98 - Towards Bioinspired Close-Loop Local Motor Control: a Simulated Approach Supporting Neuromorphic Implementations
Fernando Pérez-Peña{1}, Juan Antonio Leñero-Bardallo{1}, Alejandro Linares-Barranco{2}, Elisabetta Chicca{3}
{1}Universidad de Cádiz, Spain; {2}Universidad de Sevilla, Spain; {3}Universität Bielefeld, Germany

S-99 - Snowflake: an Efficient Hardware Accelerator for Convolutional Neural Networks
Vinayak Gokhale, Aliasger Zaidy, Andre Chang, Eugenio Culurciello
Purdue University, United States

S-100 - Extending the Neural Engineering Framework for Nonideal Silicon Synapses
Aaron Voelker{2}, Ben Benjamin{1}, Terrence Stewart{2}, Kwabena Boahen{1}, Chris Eliasmith{2}
{1}Stanford University, United States; {2}University of Waterloo, Canada

Signal Processing for Interaction & Augmented Reality
Time: Tuesday, May 30 (15:00-16:30)
Room: Harborside Ballroom
Chair(s): Susanto Rahardja - Northwestern Polytechnical University; Zicheng Liu - Microsoft Research

T-101 - D-PET: A Direct 6 DoF Pose Estimation and Tracking System on Graphics Processing Units
Hung-Yu Tseng, Po-Chen Wu, Yu-Sheng Lin, Shao-Yi Chien
National Taiwan University, Taiwan

T-102 - An Efficient DFT-Based Algorithm for the Charger Noise Problem in Capacitive Touch Applications
Shih-Lun Huang, Sheng-Yi Hung, Chung-Ping Chen
National Taiwan University, Taiwan

T-103 - Reflection Removal Based on Single Light Field Capture
Yun Ni, Jie Chen, Lap-Pui Chau
Nanyang Technological University, Singapore

T-104 - Bare-Finger Projector-Camera-Touchpad (PCT) HCI System Using Color Structured Light
Sen Li, Xiang Xie, Guolin Li, Zhihua Wang
Tsinghua University, China

T-105 - Real-Time Streaming Challenges in Internet of Video Things (IoVT)
Ahmed Sammoud{2}, Ashok Kumar{2}, Magdy Bayoumi{2}, Tarek Elarabi{1}
{1}Penn State Behrend, United States; {2}University of Louisiana at Lafayette, United States

Digital Integrated Circuits and Systems
Time: Tuesday, May 30 (15:00-16:30)
Room: Harborside Ballroom
Chair(s): Saeid Nooshabadi - Michigan Technological University

U-106 - Hardware Accelerators for Recurrent Neural Networks on FPGA
Andre Xian Ming Chang, Eugenio Culurciello
Purdue University, United States

U-107 - Residual Sampling Clocking Offset Estimation and Compensation for FBMC-OQAM Baseband Receiver in the 60 GHz Band
Chun-Yi Liu{2}, Yu-Cheng Yao{3}, Meng-Siou Sie{1}, Edmund Wen Jen Leong{1}, Henry Lopez{2}, Chih-Wei Jen{2}, Shyh-Jye Jou{2}
{1}MediaTek, Taiwan; {2}National Chiao Tung University, Taiwan; {3}Realtek Semiconductor Corp., Taiwan

U-108 - Scalable Memory-Less Architecture for String Matching with FPGAs
Ideh Sarbishei{1}, Shervin Vakili{2}, J.M. Pierre Langlois{2}, Yvon Savaria{2}
{1}École Polytechnique de Montréal, Canada; {2}Polytechnique Montréal, Canada

U-109 - Design of Majority Logic Based Approximate Arithmetic Circuits
Carson Labrado{2}, Himanshu Thapliyal{2}, Fabrizio Lombardi{1}
{1}Northeastern University, United States; {2}University of Kentucky, United States

U-110 - Noise Voltage Analysis of Spiral Inductor for on-Chip Buck Converter Design
Emeshaw Ashenafi, Masud Chowdhury
University of Missouri–Kansas City, United States

U-111 - A New Digital True Random Number Generator Based on Delay Chain Feedback Loop
Xufan Wu, Shuguo Li
Tsinghua University, China

U-112 - A Digital Clock-Less Pulse Stretcher with Application in Deep Sub-Nanosecond Pulse Detection
Zhiqiang Liu{1}, Nanqi Liu{1}, Shravan Chaganti{1}, Degang Chen{1}, Amitava Majumdar{2}
{1}Iowa State University, United States; {2}Xilinx Inc., United States

U-113 - A New Watermarking Scheme on Scan Chain Ordering for Hard IP Protection
Xiaonan Huang{1}, Aijiao Cui{1}, Chip-Hong Chang{2}
{1}Harbin Institute of Technology, China; {2}Nanyang Technological University, Singapore

U-114 - A 450kHz PVT-Resilient All-Digital BPSK Demodulator for Energy Harvesting Sensor Nodes
Adelson Chua, Louis Alarcon
University of the Philippines - Diliman, Philippines

U-115 - Single Supply CMOS Up Level Shifter for Dual Voltage System
Jose Carlos García{2}, Juan Montiel-Nelson{2}, Saeid Nooshabadi{1}
{1}Michigan Technological University, United States; {2}Universidad de Las Palmas de Gran Canaria, Spain

U-116 - Nodal Thermal Analysis for Multi-VT SOFFET Based Subthreshold Circuits
Emeshaw Ashenafi, Azzedin Es-Sakhi, Masud Chowdhury
University of Missouri–Kansas City, United States

U-117 - Trojan-Feature Extraction at Gate-Level Netlists and its Application to Hardware-Trojan Detection Using Random Forest Classifier
Kento Hasegawa, Masao Yanagisawa, Nozomu Togawa
Waseda University, Japan

U-118 - Non-Blocking BIST for Continuous Reliability Monitoring of Networks-on-Chip
Junshi Wang{3}, Letian Huang{3}, Masoumeh Ebrahimi{1}, Qiang Li{3}, Guangjun Li{3}, Axel Jantsch{2}
{1}KTH Royal Institute of Technology / University of Turku, Finland; {2}Technische Universität Wien, Austria; {3}University of Electronic Science and Technology of China, China

U-119 - Combined Packet and TDM Circuit Switching NoCs with Novel Connection Configuration Mechanism
Yong Chen, Emil Matus, Gerhard Fettweis
Technische Universität Dresden, Germany

U-120 - A Cost-Efficient Delay-Fault Monitor
Gaole Sai, Basel Halak, Mark Zwolinski
University of Southampton, United Kingdom

U-121 - Level Shifter Design for Voltage Stacking
Elnaz Ebrahimi, Rafael Possignolo, Jose Renau
University of California, Santa Cruz, United States

U-122 - 130nm Low Power Asynchronous AES Core
Nada El-Meligy{3}, Moustafa Amin{3}, Eslam Yahya{2}, Yehea Ismail{1}
{1}American University in Cairo / Zewail City of Science and Technology, Egypt; {2}American University in Cairo / Zewail City of Science and Technology / Banha University, Egypt; {3}Banha University, Egypt

U-123 - A Low-Cost Masquerade and Replay Attack Detection Method for CAN in Automobiles
Mohammad Raashid Ansari, Tom Miller, Chenghua She, Qiaoyan Yu
University of New Hampshire, United States

Communications Security
Time: Tuesday, May 30 (15:00-16:30)
Room: Harborside Ballroom
Chair(s): Weiqiang Liu - Nanjing University of Aeronautics and Astronautics; Maire O'Neill - Queens University

V-124 - Interpolation Based Wideband Beamforming Architecture
Bindi Wang, Hao Gao, Marion Matters-Kammerer, Peter Baltus
Eindhoven University of Technology, Netherlands

V-125 - Concatenated LDPC-Polar Codes Decoding Through Belief Propagation
Syed Mohsin Abbas, Youzhe Fan, Ji Chen, Chi-Ying Tsui
Hong Kong University of Science and Technology, Hong Kong

V-126 - Rate-Compatible and High-Throughput Architecture Designs for Encoding LDPC Codes
Nishil Talati{1}, Zhiying Wang{2}, Shahar Kvatinsky{1}
{1}Technion − Israel Institute of Technology, Israel; {2}University of California, Irvine, United States

V-127 - A Low-Complexity Fully Scalable Interleaver/Address Generator Based on a Novel Property of QPP Interleavers
Arash Ardakani, Mahdi Shabany
Sharif University of Technology, Iran

V-128 - FPGA-Based Strong PUF with Increased Uniqueness and Entropy Properties
Chongyan Gu, Neil Hanley, Maire O'Neill
Queen's University Belfast, United Kingdom

V-129 - Optimization of the PLL Based TRNG Design Using the Genetic Algorithm
Oto Petura, Ugo Mureddu, Nathalie Bochard, Viktor Fischer
University of Lyon, Jean Monnet University Saint-Etienne, France

V-130 - Low-Latency Hardware Architecture for Cipher-Based Message Authentication Code
Imed Ben Dhaou{2}, Tuan Nguyen Gia{3}, Pasi Liljeberg{3}, Hannu Tenhunen{1}
{1}KTH Royal Institute of Technology, Sweden; {2}Qassim University, Saudi Arabia; {3}University of Turku, Finland

V-131 - A Delay-Efficient Ring-LWE Cryptography Architecture for Biometric Security
Tuy Nguyen Tan, Hanho Lee
Inha University, Korea, South

V-132 - Secure Dynamic Authentication of Passive Assets and Passive IoTs Using Self-Powered Timers
Liang Zhou, Shantanu Chakrabartty
Washington University in St. Louis, United States

V-133 - A Reliable True Random Number Generator Based on Novel Chaotic Ring Oscillator
Yunfan Yang, Song Jia, Yuan Wang, Shaonan Zhang, Chao Liu
Peking University, China

V-134 - An Energy-Based Attack Flow for Temporal Misalignment Coutermeasures on Cryptosystems
Rodrigo Lellis{2}, Rafael Soares{2}, Adão Souza Jr.{1}
{1}Instituto Federal Sul-Rio-Grandense, Brazil; {2}Universidade Federal de Pelotas, Brazil

V-135 - Highly Secured State-Shift Local Clock Circuit to Countermeasure Against Side Channel Attack
Ali Akbar Pammu, Kwen-Siong Chong, Bah-Hwee Gwee
Nanyang Technological University, Singapore

Power Transfer & Charging Circuits
Time: Tuesday, May 30 (15:00-16:30)
Room: Harborside Ballroom
Chair(s): Hiroo Sekiya - Chiba University; Junrui Liang – Shanghai Tech University

W-136 - A Delay Time Controlled Active Rectifier with 95.3% Peak Efficiency for Wireless Power Transmission Systems
Zhongming Xue, Dan Li, Wei Gou, Lina Zhang, Shiquan Fan, Li Geng
Xi'an Jiaotong University, China

W-137 - Analysis and Implementation of Wireless Power Transfer System with Phase and Supply Modulation Control
Chao-Yen Huang, Chern-Lin Chen
National Taiwan University, Taiwan

W-138 - A 13.56 MHz One-Stage High-Efficiency 0X/1X R³ Rectifier for Implatable Medical Devices
Xinyuan Ge, Lin Cheng, Wing-Hung Ki
Hong Kong University of Science and Technology, Hong Kong

W-139 - Adaptive 6.78-MHz ISM Band Wireless Charging for Small Form Factor Receivers
Mohamed Abouzeid, Ahmet Tekin
Özyeğin University, Turkey

W-140 - A Primary-Side Output Current Estimator with Process Compensator for Flyback LED Drivers
Zong-You Hou, Zong-Ying Ho, Jhih-Cheng You, Chua-Chin Wang
National Sun Yat-Sen University, Taiwan

W-141 - High-Speed Driver for SiC MOSFET Based on Class-E Inverter
Yuchong Sun{2}, Ryoko Sugano{2}, Xiuqin Wei{1}, Takashi Hikihara{3}, Hiroo Sekiya{2}
{1}Chiba Institute of Technology, Japan; {2}Chiba University, Japan; {3}Kyoto University, Japan

W-142 - An Auxiliary Switched-Capacitor Power Converter (SCPC) Applied in Stacked Digital Architecture for Energy Utilization Enhancement
Shiquan Fan, Zhuoqi Guo, Jie Zhang, Xu Yang, Li Geng
Xi'an Jiaotong University, China

W-143 - Switch-Mode Gyrator-Based Emulated Inductor Enabling Self-Tunability in WPT Receivers
Mohamed Saad, Elisenda Bou-Balust, Eduard Alarcón-Cot
Universitat Politècnica de Catalunya, Spain

W-144 - A Vibration-Powered Bluetooth Wireless Sensor Node with Running PFC Power Conditioning
Kang Zhao, Yuheng Zhao, Junrui Liang
ShanghaiTech University, China

W-145 - On-Chip High-Voltage SPAD Bias Generation Using a Dual-Mode, Closed-Loop Charge Pump
Boyu Shen, Soumya Bose, Matthew Johnston
Oregon State University, United States

W-146 - A Regulated Charge Pump for Injecting Floating-Gate Transistors
Mir Mohammad Navidi, David Graham
West Virginia University, United States

PIONEERS OF CAS – TUESDAY, MAY 30TH

Pioneers of Circuits and Systems II
Time: Tuesday, May 30 (16:30-17:30)
Room: Grand Ballroom V-VI
Chair(s): Pamela Abshire - University of Maryland

16:30 ***A Random Walk Through Five Decades of Research in Filters and Signal Processing***
Sanjit K. Mitra
University of California, Santa Barbara, United States

17:00 ***Beyond SPICE***
Ibrahim Hajj
University of Illinois at Urbana-Champaign, United States

TECHNICAL SESSIONS – WEDNESDAY, MAY 31ST

Complex Networks & Chaos
Time: Wednesday, May 31 (8:00-9:30)
Room: Dover A
Chair(s): Michael Tse - Hong Kong Polytechnic University; Zbigniew Galias - AGH University of Science and Technology

8:00 ***Vaccinating Sis Epidemics in Networks with Zero-Determinant Strategy***
Xiaojie Li, Cong Li, Xiang Li
Fudan University, China

8:18 **Modeling Cascading Failure Propagation in Power Systems**
Xi Zhang, Choujun Zhan, and Chi K. Tse
Hong Kong Polytechnic University, Hong Kong

8:36 ***Modeling of Cascading Failures in Cyber-Coupled Power Systems***
Dong Liu, Xi Zhang, Choujun Zhan, Chi Kong Tse
Hong Kong Polytechnic University, Hong Kong

8:54 ***Optimal Resource Allocation with Node and Link Capacity Constraints in Complex Networks***
Rui Li{2}, Yongxiang Xia{2}, Chi Kong Tse{1}
{1}Hong Kong Polytechnic University, Hong Kong; {2}Zhejiang University, China

9:12 ***Full Digital Implementation of a Chaotic Time-Delay Sampled-Data System***
Ramazan Yeniçeri, Alptekin Vardar, Mustak Erhan Yalçın
Istanbul Technical University, Turkey

Circuits & Systems for Energy Harvesting
Time: Wednesday, May 31 (8:00-9:30)
Room: Dover BC
Chair(s): Dong He - Virginia Polytechnic Institute and State University; Philip X.-L. Feng - Case Western Reserve University

8:00 ***INVITED: Leveraging the Internet of Things in the Commercial Space***
Julien Stamatakis
Senseware, United States

8:18 ***How to Design Battery-Assisted Photovoltaic Switched-Inductor CMOS Charger–Supplies***
Rajiv Damodaran Prabha, Gabriel Rincón-Mora
Georgia Institute of Technology, United States

8:36 ***Energy Harvesting Circuit with Input Matching in Boundary Conduction Mode for Electromagnetic Generators***
Yudong Xu{2}, Dong Ha{2}, Ming Xu{1}
{1}FSP-Powerland Technology Inc., China; {2}Virginia Polytechnic Institute and State University, United States

8:54 ***An Ultra-Low Quiescent Current Power Management ASIC with MPPT for Vibrational Energy Harvesting***
Shiquan Fan{1}, Liuming Zhao{1}, Ran Wei{1}, Li Geng{2}, Philip X.-L. Feng{1}
{1}Case Western Reserve University, United States; {2}Xi'an Jiaotong University, China

9:12 ***A Digital Reverse Current Self-Calibration Technique in 90% High Efficiency Rectified Power Supply for Near Field Communication Through Magnetic Field Induction***
Li-Chi Lin{1}, Kuan-Yu Chen{1}, Wen-Hau Yang{1}, Ru-Yu Huang{1}, Ke-Horng Chen{1}, Ying-Hsi Lin{2}, Shian-Ru Lin{2}, Tsung-Yen Tsai{2}
{1}National Chiao Tung University, Taiwan; {2}Realtek Semiconductor Corp., Taiwan

Neuromorphic Vision
Time: Wednesday, May 31 (8:00-9:30)
Room: Grand Ballroom I
Chair(s): Fathi Salem - Michigan Statue University; Alejandro Linares-Barranco - Universidad de Sevilla

8:00 ***INVITED: Why Ai Needs Video***
Roland Memisevic
Twenty Billion Neurons GmbH, Germany

8:18 ***Spatially Supervised Recurrent Convolutional Neural Networks for Visual Object Tracking***
Guanghan Ning{3}, Zhi Zhang{3}, Chen Huang{3}, Xiaobo Ren{2}, Haohong Wang{2}, Canhui Cai{1}, Zhihai He{3}
{1}Huaqiao University, China; {2}TCL Research America, United States; {3}University of Missouri, United States

8:36 ***Neuromorphic Visual Saliency Implementation Using Stochastic Computation***
Chetan Singh Thakur{1}, Jamal Molin{1}, Tao Xiong{1}, Jie Zhang{2}, Ernst Niebur{1}, Ralph Etienne-Cummings{1}
{1}Johns Hopkins University, United States; {2}Massachusetts Institute of Technology, United States

8:54 ***Image Classification by Cellular Nonlinear Networks***
Simon Walz, Jens Müller, Ronald Tetzlaff
Technische Universität Dresden, Germany

9:12 ***Hardware Implementation of Convolutional STDP for on-Line Visual Feature Learning***
Amirreza Yousefzadeh{1}, Timothee Masquelier{2}, Teresa Serrano-Gotarredona{1}, Bernabe Linares-Barranco{1}
{1}Consejo Superior de Investigaciones Científicas / Universidad de Sevilla, Spain; {2}Massachusetts Institute of Technology, France

Adaptive Filters
Time: Wednesday, May 31 (8:00-9:30)
Room: Grand Ballroom II
Chair(s): Mrityunjoy Chakraborty - Indian Institute of Technology Kharagpur; Wei Xing Zheng - Western Sydney University

8:00 ***Modified Subband Adaptive Notch Filters for Eliminating Multiple Sinusoids with Reduced Bias and Faster Convergence***
Yasutomo Kinugasa{2}, Tapio Saramäki{4}, Yoshio Itoh{5}, Naoto Sasaoka{5}, Kazuki Shiogai{3}, Masaki Kobayshi{1}
{1}Chubu University, Japan; {2}National Institute of Technology, Mastue College, Japan; {3}National Institute of Technology, Niihama College, Japan; {4}Tampere University of Technology, Finland; {5}Tottori University, Japan

8:18 ***A Mixed-Signal Adaptive Filter for Level-Crossing Analog-to-Digital Converter***
Yuxuan Luo, Chun-Huat Heng
National University of Singapore, Singapore

8:36 ***A Block-Based Convex Combination of NLMS and ZA-NLMS for Identifying Sparse Systems with Variable Sparsity***
Bijit K. Das, Mrityunjoy Chakraborty
Indian Institute of Technology Kharagpur, India

8:54 ***A Comparison of NLMS and LMS Algorithms for Cyclostationary Input Signals***
Sheng Zhang, Wei Xing Zheng
Western Sydney University, Australia

9:12 ***A New Kernel Kalman Filter Algorithm for Estimating Time-Varying Nonlinear Systems***
Juliano Rosinha{1}, Sérgio de Almeida{1}, José Bermudez{2}
{1}Universidade Católica de Pelotas, Brazil; {2}Universidade Federal de Santa Catarina, Brazil

RF Circuits III
Time: Wednesday, May 31 (8:00-9:30)
Room: Grand Ballroom III
Chair(s): Nathan Neihart - Iowa State University; Ayman Fayed - Ohio State University

8:00 ***A 180-nW Static Power UWB IR Transmitter Front-End for Energy Harvesting Applications***
Tuomas Haapala, Mika Pulkkinen, Jarno Salomaa, Kari Halonen
Aalto University, Finland

8:18 ***Low-Power Low-Noise Amplifier IIP3 Improvement Under Consideration of the Cascode Stage***
Chun-Hsiang Chang{2}, Marvin Onabajo{1}
{1}Northeastern University, United States; {2}OmniVision Technologies Inc., United States

8:36 ***Realization of a 10 GHz PLL in IBM 130 nm SiGe BiCMOS Process for Optical Transmitter***
Kehan Zhu{2}, Sakkarapani Balagopal{1}, Xinyu Wu{3}, Vishal Saxena{3}
{1}Broadcom Ltd., United States; {2}MultiPhy, Ltd., United States; {3}University of Idaho, United States

8:54 ***EMI Common-Mode (CM) Noise Suppression from Self-Calibration of High-Speed SST Driver Using on-Chip Process Monitoring Circuit***
Khawaja Qasim Maqbool{1}, Duona Luo{1}, Guang Zhu{1}, Xingyun Luo{2}, Huichun Yu{2}, Chik Patrick Yue{1}
{1}Hong Kong University of Science and Technology, Hong Kong; {2}Huawei Technologies Co., Ltd., China

9:12 ***Highly Linear Reconfigurable Mixer Designed for Environment-Aware Receiver***
Mohammadmahdi Mohsenpour, Carlos Saavedra
Queen's University, Canada

Trust in Fabrication & Post-Silicon Adaptation for Hardware Security
Time: Wednesday, May 31 (8:00-9:30)
Room: Grand Ballroom IV
Chair(s): Aijiao Cui - Harbin Institute of Technology Shenzhen, China

8:00 ***A Guide to Graceful Aging: How Not to Overindulge in Post-Silicon Burn-in for Enhancing Reliability of Weak PUF***
Md Nazmul Islam, Vinay C Patil, Sandip Kundu
University of Massachusetts Amherst, United States

8:18 ***Privacy Leakages in Approximate Adders***
Shahrzad Keshavarz, Daniel Holcomb
University of Massachusetts Amherst, United States

8:36 ***An Overview of Hardware Intellectual Property Protection***
Jeyavijayan Rajendran
University of Texas at Dallas, United States

8:54 ***Introducing TFUE: the Trusted Foundry and Untrusted Employee Model in IC Supply Chain Security***
Yuntao Liu, Chongxi Bao, Yang Xie, Ankur Srivastava
University of Maryland, College Park, United States

9:12 ***A Secure Test Solution for Sensor Nodes Containing Crypto-Cores***
Shoaleh Hashemi Namin, Ankit Mehta, Parham Hosseinzadeh Namin, Rashid Rashidzadeh, Majid Ahmadi
University of Windsor, Canada

Analog & Digital Senses
Time: Wednesday, May 31 (8:00-9:30)
Room: Grand Ballroom VII
Chair(s): Andreas Andreou - Johns Hopkins University; Amine Bermak - Hamad Bin Khalifa University

8:00 ***In-Vivo Validation of Fully Implantable Multi-Panel Devices for Remote Monitoring of Metabolism***
Camilla Baj-Rossi{1}, Andrea Cavallini{1}, Enver G. Kilinc{1}, Francesca Stradolini{1}, Tanja Rezzonico Jost{2}, Michele Proietti{2}, Giovanni De Micheli{1}, Fabio Grassi{2}, Catherine Dehollain{1}, Sandro Carrara{1}
{1}École Polytechnique Fédérale de Lausanne, Switzerland; {2}Università della Svizzera italiana / Institute for Research in Biomedicine, Switzerland

8:18 ***High-Precision, Mixed-Signal Mismatch Measurement of Metal-Oxide-Metal Capacitors***
Danilo Bustamante{1}, Eric Swindlehurst{2}, Shiuh-Hua Wood Chiang{1}, Devon Janke{1}
{1}Brigham Young University, United States; {2}Georgia Institute of Technology, United States

8:36 ***CMOS Amperometric ADC with High Sensitivity, Dynamic Range and Power Efficiency for Air Quality Monitoring***
Haitao Li{1}, Sam Boiling{2}, Andrew J. Mason{2}
{1}Maxim Integrated Products Inc., United States; {2}Michigan State University, United States

8:54 ***A Two-Step Prediction ADC Architecture for Integrated Low Power Image Sensors***
Hang Yu{1}, Menghan Guo{1}, Shoushun Chen{1}, Wei Tang{2}
{1}Nanyang Technological University, Singapore; {2}New Mexico State University, United States

9:12 ***A PFM Based Digital Pixel with Off-Pixel Residue Measurement for Small Pitch FPAs***
Shahbaz Abbasi, Arman Galioglu, Atia Shafique, Omer Ceylan, Melik Yazici, Yasar Gurbuz
Sabanci University, Turkey

Signal Integrity & Energy Efficiency
Time: Wednesday, May 31 (8:00-9:30)
Room: Grand Ballroom VIII
Chair(s): Duncan Elliott - University of Alberta; Antonio Strollo - Università degli Studi di Napoli Federico II

8:00 ***A 4Gb/s Half-Rate DFE with Switched-Cap and IIR Summation for Data Correction***
Gyunam Jeon, Yong-Bin Kim
Northeastern University, United States

8:18 ***In-Package Spiral Inductor Characterization for High Efficiency Buck Converters***
Chen Yan, Zhihua Gan, Emre Salman
Stony Brook University, United States

8:36 ***KKT-Condition Inspired Solution of DVFS with Limited Number of Voltage Levels***
Mineo Kaneko
Japan Advanced Institute of Science and Technology, Japan

8:54 ***A 0.2V 2.3pJ/Cycle 28dB Output SNR Hybrid Markov Random Field Probabilistic-Based Circuit for Noise Immunity and Energy Efficiency***
Xuwei Jin, Wei Jin, Hao Zhang, Jianfei Jiang, Weifeng He
Shanghai Jiao Tong University, China

9:12 ***Design of Clock Generation Circuitry for High-Speed Subranging Time-Interleaved ADCs***
Seyed Alireza Zahrai{2}, Nicolas Le Dortz{1}, Marvin Onabajo{2}
{1}Analog Devices Inc., United States; {2}Northeastern University, United States

Wearable Sensors, Circuits & Systems
Time: Wednesday, May 31 (8:00-9:30)
Room: Grand Ballroom IX
Chair(s): Wouter Serdijn - Delft University of Technology; Zhihua Wang - Tsinghua University

8:00 ***Electromechanical Cardiac Monitoring SoC for Atrial Fibrillation Detection***
Jonas Eriksson, Mika Kutila, Tapani Nevalainen, Phong Nguyen, Kati Sairanen, Marko Ylitolva, Tero Koivisto, Mikko Pänkäälä
University of Turku, Finland

8:18 ***Structured Electronic Design of High-Pass ΣΔ Converters and Their Application to Cardiac Signal Acquisition***
Samprajani Rout, Wouter Serdijn
Technische Universiteit Delft, Netherlands

8:36 ***Wearable Wireless Sensor Patch for Continuous Monitoring of Skin Temperature, Pressure, and Relative Humidity***
John McNeill{3}, Devdip Sen{3}, Yitzhak Mendelson{3}, Matthew Crivello{1}, Shamsur Mazumder{3}, Amanda Agdeppa{3}, Syed Ali Hussain{3}, Hyunsoo Kim{3}, Victoria Loehle{3}, Raymond Dunn{2}, Kelli Hickle{2}
{1}Analog Devices Inc., United States; {2}University of Massachusetts Medical School, United States; {3}Worcester Polytechnic Institute, United States

8:54 ***Ultrasound Sensors and its Application in Human Heart Rate Monitoring***
Amirhossein Shahshahani{1}, Davood Raeisi Nafchi{2}, Zeljko Zilic{1}
{1}McGill University, Canada; {2}Tehran University, Iran

9:12 ***Design and Parametric Analysis of a Wearable Dual-Photoplethysmograph Based System for Pulse Wave Velocity Detection***
Zachary Trujillo, Viswam Nathan, Gerard Coté, Roozbeh Jafari
Texas A&M University, United States

Filter Design
Time: Wednesday, May 31 (8:00-9:30)
Room: Grand Ballroom X
Chair(s): Igor Filanvosky - University of Alberta; Nuno Paulino - UNINOVA

8:00 ***Property of Rational Functions Related to Band-Pass Transformation with Application to Symmetric Filters Design***
Igor Filanovsky
University of Alberta, Canada

8:18 ***Analysis of Second-Order Intermodulation in Miller Bandpass Filters***
Joung Won Park{1}, Behzad Razavi{2}
{1}Qualcomm Technologies, Inc., United States; {2}University of California, Los Angeles, United States

8:36 ***A New 2nd–Order Allpass Filter in 130nm CMOS***
Brent Maundy{2}, Peyman Ahmadi{2}, Ahmed Elwakil{3}, Leonid Belostotski{2}, Arjuna Madanayake{1}
{1}University of Akron, United States; {2}University of Calgary, Canada; {3}University of Sharjah, U.A.E.

8:54 ***A 50 Hz SC Notch Filter for IoT Applications***
Hugo Serra, João Pedro Oliveira, Nuno Paulino
Universidade Nova de Lisboa / CTS-UNINOVA, Portugal

Error Correcting Codes
Time: Wednesday, May 31 (8:00-9:30)
Room: Laurel AB
Chair(s): Zhiyuan Yan - Lehigh University; Xinmiao Zhang - Case Western University

8:00 ***A Fast Polar Code List Decoder Architecture Based on Sphere Decoding***
Seyyed Ali Hashemi, Carlo Condo, Warren Gross
McGill University, Canada

8:18 ***Efficient Metric Sorting Schemes for Successive Cancellation List Decoding of Polar Codes***
Haochuan Song{2}, Shunqing Zhang{1}, Xiaohu You{2}, Chuan Zhang{2}
{1}Intel Corporation, China; {2}Southeast University, China

8:36 ***Low-Complexity Transformed Encoder Architectures for Quasi-Cyclic Nonbinary LDPC Codes Over Subfields***
Xinmiao Zhang, Ying Tai
Western Digital, United States

8:54 ***Efficient Approximate Layered LDPC Decoder***
Yangcan Zhou, Jun Lin, Zhongfeng Wang
Nanjing University, China

9:12 ***Symmetric Split-Row LDPC Decoders***
Mohammad Shahrad{1}, Mahdi Shabany{2}
{1}Princeton University, United States; {2}Sharif University of Technology, Iran

Design for Test & Manufacturability
Time: Wednesday, May 31 (8:00-9:30)
Room: Laurel CD
Chair(s): Ricardo Reis - Federal University of Rio Grande do Su; Massimo Alioto - NTU

8:00 ***Design-Oriented Models for Quick Estimation of Path Delay Variability via the Fan-Out-of-4 Metric***
Massimo Alioto{1}, Giuseppe Scotti{2}, Alessandro Trifiletti{2}
{1}National University of Singapore, Singapore; {2}Sapienza – Università di Roma, Italy

8:18 ***A Secure Scan Chain Test Scheme Exploiting Retention Loss of Memristors***
Yanping Gong, Fengyu Qian, Lei Wang
University of Connecticut, United States

8:36 ***Layout Decomposition for Hybrid E-Beam and DSA Double Patterning Lithography***
Yunfeng Yang{1}, Fan Yang{1}, Wai-Shing Luk{1}, Changhao Yan{1}, Xuan Zeng{1}, Xiangdong Hu{2}
{1}Fudan University, China; {2}Shanghai High-Performance Integrated-Circuit Design Center, China

8:54 ***Test Pattern Generation for Multiple Stuck-at Faults Not Covered by Test Patterns for Single Faults***
Conrad Moore, Peikun Wang, Amir Masoud Gharehbaghi, Masahiro Fujita
University of Tokyo, Japan

9:12 ***A New Approach for Diagnosing Bridging Faults in Logic Designs***
Amir Masoud Gharehbaghi, Masahiro Fujita
University of Tokyo, Japan

CAS-T papers on Memory
Time: Wednesday, May 31 (8:00-9:30)
Room: Kent AB
Chair(s): Pierre-Emmanuel Gaillardon - University of Utah; Lan-Da Van - National Chiao Tung University

8:00 ***A Study on the Programming Structures for RRAM-Based FPGA Architectures***
Xifan Tang{1}, Gain Kim{1}, Giovanni De Micheli{1}, Pierre-Emmanuel Gaillardon{2}
{1}École Polytechnique Fédérale de Lausanne, Switzerland; {2}University of Utah, United States

8:18 ***Reconfigurable Writing Architecture for Reliable RRAM Operation in Wide Temperature Ranges***
Fernando García-Redondo, Pablo Royer, Marisa López-Vallejo, Hernan Aparicio, Pablo Ituero, Carlos López-Barrio
Universidad Politécnica de Madrid, Spain

8:36 ***PEVA: a Page Endurance Variance Aware Strategy for the Lifetime Extension of NAND Flash***
Debao Wei, Liyan Qiao, Peng Zhang, Xiyuan Peng, Libao Deng
Harbin Institute of Technology, China

8:54 ***28-nm 1T-1MTJ 8Mb 64 I/O STT-MRAM with Symmetric 3-Section Reference Structure and Cross-Coupled Sensing Amplifier***
Artur Antonyan, Suksoo Pyo, Hyuntaek Jung, Gwan-Hyeob Koh, Taejoong Song
Samsung Electronics, Korea, South

Mini-Tutorial
Time: Wednesday, May 31 (8:00-9:30)
Room: Essex AB

8:00 ***Dynamic Comparator Noise and Metastability Simulation Techniques***
William Evans
Cadence Design Systems, United States

Awards Ceremony and Keynote
Time: Wednesday, May 31 (10:00-11:45)
Room: Grand Ballroom V-VI

10:00 ***Awards Ceremony***
IEEE Ibuka Award
IEEE CAS Society Awards, IEEE CASS Student Design Competition
ISCAS 2017 Awards

10:45 ***Unleashing the Promise of the Internet of Things***
Tyson Tuttle, President and CEO, Silicon Labs

Spintronic-based Technology
Time: Wednesday, May 31 (13:30-15:00)
Room: Dover A
Chair(s): Malgorzata Chrzanows-Jeske - Portland State University; Mircea Stan - University of Virginia

13:30 ***Energy-Efficient Magnetic Circuits Based on Nanoelectronic Devices***
Fazel Sharifi, Himanshu Thapliyal
University of Kentucky, United States

13:48 ***A Variation-Aware Simulation Framework for Hybrid CMOS/Spintronic Circuits***
Raffaele De Rose{6}, Marco Lanuzza{6}, Felice Crupi{6}, Giulio Siracusano{3}, Riccardo Tomasello{5}, Giovanni Finocchio{4}, Mario Carpentieri{2}, Massimo Alioto{1}
{1}National University of Singapore, Singapore; {2}Politecnico di Bari, Italy; {3}Università degli Studi di Catania, Italy; {4}Università degli Studi di Messina, Italy; {5}Università degli Studi di Perugia, Italy; {6}Università della Calabria, Italy

14:06 ***Hybrid Polymorphic Logic Gate Using 6 Terminal Magnetic Domain Wall Motion Device***
Farhana Parveen, Shaahin Angizi, Zhezhi He, Deliang Fan
University of Central Florida, United States

14:24 ***Rectified-Linear and Recurrent Neural Networks Built with Spin Devices***
Qing Dong, Kaiyuan Yang, Laura Fick, David Blaauw, Dennis Sylvester
University of Michigan, United States

14:42 ***Cross-Layer Design and Analysis of a Low Power, High Density STT-MRAM for Embedded System***
Manu Komalan{1}, Sushil Sakhare{1}, Trong Huynh Bao{1}, Siddharth Rao{1}, Woojin Kim{1}, Christian Tenllado{2}, Jose Ignaico Gómez{2}, Gouri Sankar Kar{1}, Arnaud Furnemont{1}, Francky Catthoor{1}
{1}IMEC, Belgium; {2}Universidad Complutense de Madrid, Spain

Energy Grids & Systems
Time: Wednesday, May 31 (13:30-15:00)
Room: Dover BC
Chair(s): Chika Nwankpa - Drexel University; Xiaozhe Wang - McGill University

13:30 ***Implementation of Power Factor Corrector with Fractional Capacitor***
Yuehai Lu, Dongyuan Qiu, Bo Zhang, Yanfeng Chen, Yanwei Jiang
South China University of Technology, China

13:48 ***Subsystem Size Optimization for Efficient Parallel Restoration of Power Systems***
Nuwan Ganganath{1}, Chi-Tsun Cheng{1}, Herbert Ho-Ching Iu{2}, Tyrone Fernando{2}
{1}Hong Kong Polytechnic University, Hong Kong; {2}University of Western Australia, Australia

14:06 ***PMU-Based Estimation of Dynamic State Jacobian Matrix***
Xiaozhe Wang{2}, Konstantin Turitsyn{1}
{1}Massachusetts Institute of Technology, United States; {2}McGill University, Canada

14:24 ***Battery Energy Storage Dispatch Analysis Within the Storage Placement Problem***
Jesse Hill, Chika Nwankpa
Drexel University, United States

14:42 ***Adaptive Droop Control with Self-Adjusted Virtual Impedance for Three-Phase Inverter Under Unbalanced Conditions***
Zelun Lu{1}, Wenxuan Li{1}, Zhen Li{1}, Xi Chen{2}, Herbert Ho-Ching Iu{3}, Ning Dong{1}, Xiangdong Liu{1}
{1}Beijing Institute of Technology, China; {2}Global Energy Interconnection Research Institute North America, United States; {3}University of Western Australia, Australia

Brain Inspired Circuits and Systems
Time: Wednesday, May 31 (13:30-15:00)
Room: Grand Ballroom I
Chair(s): Sankar Basu - National Science Foundation; Mona Zaghloul - George Washington University

13:30 ***INVITED: Implications of a Spontaneously Active Ground State for Computing with Brain-Inspired Circuits***
Narayan Srinivasa
Intel Corporation, United States

13:48 ***Demonstrating Hybrid Learning in a Flexible Neuromorphic Hardware System***
Simon Friedmann, Johannes Schemmel, Andreas Grübl, Andreas Hartel, Matthias Hock, Karlheinz Meier
Ruprecht-Karls-Universität Heidelberg, Germany

14:06 ***Calibrating Silicon-Synapse Dynamics Using Time-Encoding and Decoding Machines***
Eric Kauderer-Abrams, Kwabena Boahen
Stanford University, United States

14:24 ***Path Planning on the TrueNorth Neurosynaptic System***
Kate Fischl{2}, Kaitlin Fair{1}, Wei-Yu Tsai{3}, Jack Sampson{3}, Andreas G. Andreou{2}
{1}Georgia Institute of Technology, United States; {2}Johns Hopkins University, United States; {3}Pennsylvania State University, United States

14:42 ***Low-Power, Low-Mismatch, Highly-Dense Array of VLSI Mihalas-Niebur Neurons***
Jamal Molin{2}, Adebayo Eisape{2}, Chetan Singh Thakur{2}, Vigil Varghese{3}, Christian Brandli{1}, Ralph Etienne-Cummings{2}
{1}Insightness AG, Switzerland; {2}Johns Hopkins University, United States; {3}Nanyang Technological University, Singapore

Digital Filters & Filter Banks
Time: Wednesday, May 31 (13:30-15:00)
Room: Grand Ballroom II
Chair(s): Tapio Saramaki - Tampere University of Technology; Zhiping Lin - Nanyang Technological University

13:30 ***Roundoff Noise Minimization for 2-D Separable-Denominator Digital Filters Using Jointly Optimal High-Order Error Feedback and Realization***
Takao Hinamoto{2}, Akimitsu Doi{1}, Wu-Sheng Lu{3}
{1}Hiroshima Institute of Technology, Japan; {2}Hiroshima University, Japan; {3}University of Victoria, Canada

13:48: ***Design of IIR Frequency-Response Masking Filters with Near Linear Phase Using Constrained Optimization***
Qinglai Liu{2}, Yong Ching Lim{2}, Zhiping Lin{2}, Xiaoping Lai{1}
{1}Hangzhou Dianzi University, China; {2}Nanyang Technological University, Singapore

14:06 ***FPGA Implementation of 2-D Wave Digital Filters for Real Time Motion Feature Extraction***
Lech Kolonko, Joerg Velten, Daniel Wagner, Anton Kummert
Bergische Universität Wuppertal, Germany

14:24 ***Design of Cascaded Integrator-Comb Decimation Filters for Direct-RF Sampling Receivers***
Takao Kihara, Hiroyuki Yano, Tsutomu Yoshimura
Osaka Institute of Technology, Japan

14:42 ***Design of Orthogonal Filterbanks with Rational Coefficients Using Gröbner Bases***
Nhu Y Le{4}, Zhiping Lin{4}, David Tay{3}, Li Xu{1}, Jiuwen Cao{2}
{1}Akita Prefectural University, Japan; {2}Hangzhou Dianzi University, China; {3}La Trobe University, Australia; {4}Nanyang Technological University, Singapore

Wireless Power & Data Transfer to Biomedical Implants
Time: Wednesday, May 31 (13:30-15:00)
Room: Grand Ballroom III
Chair(s): Pedram Mohseni - Case Western Reserve; Mehdi Kiani - Pennsylvania State University

13:30 ***Inductive and Ultrasonic Wireless Power Transmission to Biomedical Implants***
Ahmed Ibrahim, Miao Meng, Mehdi Kiani
Pennsylvania State University, United States

13:48 ***Transcutaneous Capacitive Wireless Power Transfer (C–WPT) for Biomedical Implants***
Reza Erfani{1}, Fatemeh Marefat{1}, Amir Sodagar{2}, Pedram Mohseni{1}
{1}Case Western Reserve University, United States; {2}Khajeh Nasir Toosi University of Technology, Iran

14:06 ***A Wirelessly Powered High-Speed Transceiver for High-Density Bidirectional Neural Interfaces***
Esmaeel Maghsoudloo, Masoud Rezaei, Benoit Gosselin
Université Laval, Canada

14:24 ***Design and Modeling of an Inductive Coupling Wireless Power Transfer Using Printed Spirals on Medical Hydrocolloid Dressings***
Haneen Alsuradi{1}, Jerald Yoo{2}
{1}Masdar Institute of Science and Technology, U.A.E.; {2}Masdar Institute of Science and Technology / National University of Singapore, Singapore

14:42 ***INVITED: Wireless Power Transfer: Far Field to Near Field***
Zohaib Hameed, Kambiz Moez
3M Corporate Research Laboratories–SEMS, United States

3D Integrated Circuits
Time: Wednesday, May 31 (13:30-15:00)
Room: Grand Ballroom IV
Chair(s): Eby Friedman - University of Rochester; Hassan Mostafa - University of Waterloo

13:30 ***Hybrid Energy Harvesting in 3-D IC IoT Devices***
Boris Vaisband, Eby G. Friedman
University of Rochester, United States

13:48 ***Fault Tolerant Techniques for TSV-Based Inteconnects in 3-D ICs***
Siroos Madani{2}, Magdy Bayoumi{1}
{1}University of Louisiana at Lafayette, United States; {2}University of Louisina, United States

14:06 ***Open Source Cell Library Mono3D to Develop Large-Scale Monolithic 3D Integrated Circuits***
Chen Yan, Scott Kontak, Hailang Wang, Emre Salman
Stony Brook University, United States

14:24 ***Contactless Inter-Tier Communication for Heterogeneous 3-D ICs***
Ioannis Papistas, Vasilis Pavlidis
University of Manchester, United Kingdom

14:42 ***Runtime Energy Management Under Real-Time Constraints in MPSoCs***
André Martins, Marcelo Ruaro, Anderson Santana, Fernando Moraes
Pontifícia Universidade Católica do Rio Grande do Sul, Brazil

Analog Signal Processing
Time: Wednesday, May 31 (13:30-15:00)
Room: Grand Ballroom VII
Chair(s): Filippo Neri - u-blox, Switzerland; Nuno Paulino - UNINOVA

13:30 ***A High-Speed and Ultra Low-Power Subthreshold Signal Level Shifter***
Esmaeel Maghsoudloo{2}, Masoud Rezaei{2}, Benoit Gosselin{2}, Mohamad Sawan{1}
{1}Polytechnique Montréal, Canada; {2}Université Laval, Canada

13:48 ***Analysis and Design of the Classical CMOS Schmitt Trigger in Subthreshold Operation***
Luiz Alberto Pasini Melek, Anselmo Luís da Silva Jr., Márcio Cherem Schneider, Carlos Galup-Montoro
Universidade Federal de Santa Catarina, Brazil

14:06 ***A Low Power Analog Voltage Similarity Circuit***
Mehdi Azadmehr, Luca Marchetti, Yngvar Berg
University College of SouthEast Norway, Norway

14:24 ***Chopping in Continuous-Time Sigma-Delta Modulators***
Hui Jiang, Burak Gönen, Kofi Makinwa, Stoyan Nihitanov
Technische Universiteit Delft, Netherlands

14:42 ***On Linear Periodically Time Varying (LPTV) Systems with Modulated Inputs, and Their Application to Smoothing Filters***
Shanthi Pavan
Indian Institute of Technology Madras, India

Biosignal Amplifiers
Time: Wednesday, May 31 (13:30-15:00)
Room: Grand Ballroom IX
Chair(s): Timothy Constandinou - Imperial College London; Ross M Walker - Michigan State University

13:30 ***Two-Electrode Impedance-Sensing Cardiac Rhythm Monitor for Charge-Aware Shock Delivery in Cardiac Arrest***
M. Reza Pazhouhandeh{2}, Omid Shoaei{1}, Roman Genov{2}
{1}University of Tehran, Iran; {2}University of Toronto, Canada; {2}University of Toronto, Iran

13:48 ***A 16-Channel CMOS Chopper-Stabilized Analog Front-End Acquisition Circuits for ECoG Detection***
Cheng-Hsiang Cheng, Zhi-Xin Chen, Chung-Yu Wu
National Chiao Tung University, Taiwan

14:06 ***A Noise-Power-Area Optimized Novel Programmable Gain and Bandwidth Instrumentation Amplifier for Biomedical Applications***
Devarshi Mrinal Das, Abhishek Srivastava, Aman Gupta, Kashyap Barot, Maryam Shojaei Baghini
Indian Institute of Technology Bombay, India

14:24 ***A 0.5V Time-Domain Instrumentation Circuit with Clocked and Unclocked ΔΣ Operation***
Lieuwe Leene, Timothy Constandinou
Imperial College London, United Kingdom

14:42 ***An ECG Chopper Amplifier Achieving 0.92 NEF and 0.85 PEF with AC-Coupled Inverter-Stacking for Noise Efficiency Enhancement***
Somok Mondal, Drew A. Hall
University of California, San Diego, United States

Regulators & References
Time: Wednesday, May 31 (13:30-15:00)
Room: Grand Ballroom X
Chair(s): Ayman Fayed - Ohio State University; Nathan Neihart - Iowa State University

13:30 ***Low Power Output-Capacitorless Class-AB CMOS LDO Regulator***
Vahideh Shirmohammadli{2}, Alireza Saberkari{2}, Herminio Martínez-García{1}, Eduard Alarcón-Cot{1}
{1}Universitat Politècnica de Catalunya, Spain; {2}University of Guilan, Iran

13:48 ***A 276nW, Area-Eficient CMOS Subbandgap Reference Circuit***
Vahid Mohammadi Bonehi, Soheil Aghaie, Kai Hussmann, Ralf Wunderlich, Stefan Heinen
Rheinisch-Westfälische Technische Hochschule Aachen, Germany

14:06 ***A Multi-Phase VCO Quantizer Based Adaptive Digital LDO in 65nm CMOS Technology***
Somnath Kundu, Chris H. Kim
University of Minnesota Twin Cities, United States

14:24 ***Transient-Enhanced Output-Capacitorless CMOS LDO Regulator for Battery-Operated Systems***
Jorge Pérez-Bailón, Alejandro Márquez, Belén Calvo, Nicolás Medrano
Universidad de Zaragoza, Spain

Memristor-Based Technology & Circuits I
Time: Wednesday, May 31 (13:30-15:00)
Room: Laurel AB
Chair(s): Yeong-Kang Lai - National Chung Hsing University; Meng-Fan Chang - National Tsing Hua University

13:30 ***Computation of Boolean Matrix Chain Products in 3D ReRAM***
Alvaro Velasquez, Sumit Jha
University of Central Florida, United States

13:48 ***An RF Memristor Model and Memristive Single-Pole Double-Throw Switches***
Nicolas Wainstein, Shahar Kvatinsky
Technion – Israel Institute of Technology, Israel

14:06 ***A Memristor-CMOS Hybrid Architecture Concept for on-Line Template Matching***
Alexantrou Serb{2}, Christos Papavassiliou{1}, Themistoklis Prodromakis{2}
{1}Imperial College London, United Kingdom; {2}University of Southampton, United Kingdom

14:24 ***Design of Compact Memristive in-Memory Computing Systems Using Model Counting***
Dwaipayan Chakraborty, Sumit Kumar Jha
University of Central Florida, United States

14:42 ***Cell-to-Array Thermal-Aware Analysis of Stacked RRAM***
Yingyi Luo, Seda Ogrenci-Memik, Jie Gu
Northwestern University, United States

Logic Circuits & Synthesis
Time: Wednesday, May 31 (13:30-15:00)
Room: Laurel CD
Chair(s): Kwen-Siong Chong - Nanyang Technological University; Ricardo Reis - Federal University of Rio Grande do Su

13:30 ***Publish-Subscribe Programming for a NoC-Based Multiprocessor System-on-Chip***
Jean Carlo Hamerski{1}, Geancarlo Abich{2}, Ricardo Reis{2}, Luciano Ost{3}, Alexandre Amory{1}
{1}Pontifícia Universidade Católica do Rio Grande do Sul, Brazil; {2}Universidade Federal do Rio Grande do Sul, Brazil; {3}University of Leicester, United Kingdom

13:48 ***Highly Parallel Bitmap-Based Regular Expression Matching for Text Analytics***
Xuan-Thuan Nguyen{3}, Hong-Thu Nguyen{3}, Katsumi Inoue{1}, Osamu Shimojo{2}, Cong-Kha Pham{3}
{1}Advanced Original Technologies Co., Ltd., Japan; {2}Nippon Computer Dynamics Co., Ltd, Japan; {3}University of Electro-Communications, Japan

14:06 ***Memory Partitioning-Based Modulo Scheduling for High-Level Synthesis***
Tianyi Lu, Shouyi Yin, Xianqing Yao, Zhicong Xie, Leibo Liu, Shaojun Wei
Tsinghua University, China

14:24 ***Search Space Reduction for the Non-Exact Projective NPNP Boolean Matching Problem***
Feng Wang, Jiaxi Zhang, Lange Wu, Wentai Zhang, Guojie Luo
Peking University, China

14:42 ***A 50Gb/s Repeater and 2×50Gb/s 2^7-1 PRBS Generator***
Dengrong Li, Liji Wu, Shuai Yuan, Xiangmin Zhang
Tsinghua University, China

Memory: DRAM, SRAM, ReRAM, Flash, Racetrack
Time: Wednesday, May 31 (13:30-15:00)
Room: Kent AB
Chair(s): Daniele Ielmini - Politecnico di Milano; Sorin Cotofana - Delft University of Technology

13:30 ***Area and Energy-Efficient Complementary Dual-Modular Reduncdancy Dynamic Memory for Space Applications***
Robert Giterman, Lior Atias, Adam Teman
Bar-Ilan University, Israel

13:48 ***Alternative Architectures Towards Reliable Memristive Crossbar Memories***
Ioannis Vourkas{1}, Dimitrios Stathis{1}, Georgios Ch. Sirakoulis{1}, Said Hamdioui{2}
{1}Democritus University of Thrace, Greece; {2}Technische Universiteit Delft, Netherlands

14:06 ***Fixation Ratio of Error Location-Aware Strategy for Increased Reliable Retention Time of Flash Memory***
Debao Wei, Liyan Qiao, Shiyuan Wang, Xiyuan Peng
Harbin Institute of Technology, China

14:24 ***Domain Wall Racetrack Memory for in Memory Computing***
Kejie Huang{2}, Rong Zhao{1}
{1}Singapore University of Technology and Design, Singapore; {2}Zhejiang University, China

Spiking & Event-Based Systems I
Time: Wednesday, May 31 (15:15-16:45)
Room: Dover A
Chair(s): Majid Ahmadi - University of Windsor; Chiara Bartolozzi - Istituto Italiano di Tecnologia

15:15 ***Obstacle Avoidance with LGMD Neuron: Towards a Neuromorphic UAV Implementation***
Llewyn Salt{2}, Giacomo Indiveri{1}, Yulia Sandamirskaya{1}
{1}Universität Zürich / Eidgenössische Technische Hochschule Zürich, Switzerland; {2}University of Queensland, Australia

15:33 ***Pipeline AER Arbitration with Event Aging***
Juan Antonio Leñero-Bardallo{2}, Fernando Pérez-Peña{2}, Ricardo Carmona-Galán{1}, Ángel Rodríguez-Vázquez{1}
{1}Consejo Superior de Investigaciones Científicas / Universidad de Sevilla, Spain; {2}Universidad de Cádiz, Spain

15:51 ***Integer Factorization with a Neuromorphic Sieve***
John Monaco, Manuel Vindiola
U.S. Army Research Laboratory, United States

16:09 ***INVITED: Synaptic Integrators Implement Inhibitory Plasticity, Eliminate Loops and Create a "Winnerless" Network***
James Kozloski
IBM Research, United States

16:27 ***Ring Oscillator Based Sub-1V Leaky Integrate-and-Fire Neuron Circuit***
Bibhu Datta Sahoo
University of Illinois at Urbana-Champaign, United States

Neuromorphic Circuits & Systems for Robotics
Time: Wednesday, May 31 (15:15-16:45)
Room: Dover BC
Chair(s): Scott Koziol - Baylor University; Jeff Krichmar - University of California, Irvine

15:15 ***A Complete Neuromorphic Solution to Outdoor Navigation and Path Planning***
Tiffany Hwu, Jeffrey Krichmar, Xinyun Zou
University of California, Irvine, United States

15:33 ***Effect of Synaptic Charge Convergence on Path Planning Over a Neural Network***
Shashikant Koul, Timothy Horiuchi
University of Maryland, College Park, United States

15:51 ***Towards a Neuromorphic Implementation of Hierarchical Temporal Memory on SpiNNaker***
Florian Walter, Marwin Sandner, Florian Röhrbein, Alois Knoll
Technische Universität München, Germany

16:09 ***Obstacle Avoidance and Target Acquisition in Mobile Robots Equipped with Neuromorphic Sensory-Processing Systems***
Moritz Milde{1}, Alexander Dietmüller{1}, Hermann Blum{1}, Giacomo Indiveri{2}, Yulia Sandamirskaya{2}
{1}Eidgenössische Technische Hochschule Zürich, Switzerland; {2}Universität Zürich / Eidgenössische Technische Hochschule Zürich, Switzerland

16:27 ***A Population-Level Approach to Temperature Robustness in Neuromorphic Systems***
Eric Kauderer-Abrams{1}, Andrew Gilbert{1}, Aaron Voelker{2}, Ben Benjamin{1}, Terrence Stewart{2}, Kwabena Boahen{1}
{1}Stanford University, United States; {2}University of Waterloo, Canada

Emerging Technologies in Neural System Implementations
Time: Wednesday, May 31 (15:15-16:45)
Room: Grand Ballroom I
Chair(s): Chiara Bartolozzi - Istituto Italiano di Tecnologia; Jim Harkin - Ulster University

15:15 ***INVITED: Cognitive Computing Revolution: the Transformation of Embedded Neural Network Systems***
Chris Rowen
Cognite Ventures, United States

15:33 ***Associative Search Using Pseudo-Analog Memristors***
Mika Laiho{2}, Mika Grönroos{2}, Jussi Poikonen{2}, Eero Lehtonen{2}, Reon Katsumura{1}, Atsushi T. Fukuchi{1}, Masashi Arita{1}, Yasuo Takahashi{1}
{1}Hokkaido University, Japan; {2}University of Turku, Finland

15:51 ***Mitigating Noise Effects in Volatile Nano-Metal Oxide Neural Detector***
Isha Gupta, Alexantrou Serb, Ali Khiat, Themistoklis Prodromakis
University of Southampton, United Kingdom

16:09 ***Reducing Circuit Design Complexity for Neuromorphic Machine Learning Systems Based on Non-Volatile Memory Arrays***
Pritish Narayanan{2}, Lucas L. Sanches{2}, Alessandro Fumarola{2}, Robert M. Shelby{2}, Stefano Ambrogio{2}, Junwoo Jang{2}, Hyunsang Hwang{3}, Yusuf Leblebici{1}, Geoffrey W. Burr{2}
{1}École Polytechnique Fédérale de Lausanne, Switzerland; {2}IBM Research, United States; {3}Pohang University of Science and Technology, Korea, South

16:27 ***Nonlinear Dynamics of Memristor Oscillators via the Flux–Charge Analysis Method***
Fernando Corinto{1}, Mauro Forti{2}
{1}Politecnico di Torino, Italy; {2}Università degli Studi di Siena, Italy

Image Processing
Time: Wednesday, May 31 (15:15-16:45)
Room: Grand Ballroom II
Chair(s): Omair Ahmed - Concordia University; Kai-Kuang Ma - Nanyang Technological University

15:15 ***Patch-Based Salient Region Detection Using Statistical Modeling in the Non-Subsampled Contourlet Domain***
Masoumeh Rezaie Abkenar, Hamidreza Sadreazami, M. Omair Ahmad
Concordia University, Canada

15:33 ***Fast Image Super-Resolution via Randomized Multi-Split Forests***
Zhi-Song Liu, Wan-Chi Siu, Yui-Lam Chan
Hong Kong Polytechnic University, Hong Kong

15:51 ***Data-Adaptive Color Image Denoising and Enhancement Using Graph-Based Filtering***
Hamidreza Sadreazami, Amir Asif, Arash Mohammadi
Concordia University, Canada

16:09 ***Document Image Binarization via Optimized Hybrid Thresholding***
Yunfeng Liang{3}, Zhiping Lin{3}, Lei Sun{1}, Jiuwen Cao{2}
{1}Beijing Institute of Technology, China; {2}Hangzhou Dianzi University, China; {3}Nanyang Technological University, Singapore

16:27 ***Single Underwater Image Restoration Using Attenuation-Curve Prior***
Yi Wang, Hui Liu, Lap-Pui Chau
Nanyang Technological University, Singapore

Low Power Digital Circuits
Time: Wednesday, May 31 (15:15-16:45)
Room: Grand Ballroom III
Chair(s): Jun Zhou - Agency for Science, Technology and Research; Fengbo Ren - Arizona State University

15:15 ***Power-Precision Scalable Latch Memories***
Darjn Esposito{2}, Antonio Strollo{2}, Massimo Alioto{1}
{1}National University of Singapore, Singapore; {2}Università degli Studi di Napoli Federico II, Italy

15:33 ***Adiabatic Capacitive Logic: a Paradigm for Low-Power Logic***
Gael Pillonnet{2}, Herve Fanet{2}, Samer Houri{1}
{1}Technische Universiteit Delft, Netherlands; {2}Université Grenoble Alpes / Commissariat à l'énergie atomique et aux énergies alternatives, France

15:51 ***Transistor Sizing Strategy for Simultaneous Energy-Delay Optimization in CMOS Buffers***
Longyang Lin, Kien Trinh Quang, Massimo Alioto
National University of Singapore, Singapore

16:09 ***Evaluation of Dual Mode Logic in 28nm FD-SOI Technology***
Ramiro Taco{2}, Itamar Levi{1}, Marco Lanuzza{2}, Alexander Fish{1}
{1}Bar-Ilan University, Israel; {2}Università della Calabria, Italy

16:27 ***A 0.4V 0.08fJ/Cycle Retentive True-Single-Phase-Clock 18T Flip-Flop in 28nm FDSOI CMOS***
François Stas, David Bol
Université Catholique de Louvain, Belgium

Oscillators, Phase-locked Loops & Others II
Time: Wednesday, May 31 (15:15-16:45)
Room: Grand Ballroom IV
Chair(s): Igor Filanvosky - University of Alberta; Degang Chen - Iowa State University

15:15 ***Design of a Low-Jitter Wideband Frequency Synthesizer for 802.11ad Wireless OFDM Systems Using a Frequency Sixtupler***
Frank Herzel, Arzu Ergintav, Johannes Borngraeber, Herman Jalli Ng, Dietmar Kissinger
IHP GmbH, Germany

15:33 ***Optimum Scaling of Stages in a Frequency Divider Chain for Best Jitter FoM***
Sumit Kumar, Nagendra Krishnapura
Indian Institute of Technology Madras, India

15:51 ***A 0.4V 4.8µW 16MHz CMOS Crystal Oscillator Achieving 74-Fold Startup-Time Reduction Using Momentary Detuning***
Ka-Meng Lei, Pui-In Mak, Rui Paulo Martins
University of Macau, Macau

16:09 ***Phase-Locked Loops Using Switched-Gain Control***
Haixiang Zhao, Soumyajit Mandal
Case Western Reserve University, United States

16:27 ***A 69-Mbps Dual Tuning 8PSK/QPSK Transmitter Using Injection Locking and RF Phase Modulation***
Zina Saheb, Ezz El-Masry, Jean-Francois Bousquet
Dalhousie University, Canada

Sensory Circuits & Systems
Time: Wednesday, May 31 (15:15-16:45)
Room: Grand Ballroom VII
Chair(s): Amine Bermak - Hamad Bin Khalifa University; Timothy Constandinou - Imperial College London

15:15 ***462-nW 2-Axis Gesture Sensor Interface Based on Capacitively Controlled Ring Oscillators***
Mika Pulkkinen, Jarno Salomaa, Mohammad Mehdi Moayer, Tuomas Haapala, Kari Halonen
Aalto University, Finland

15:33 ***Dual Transduction Gas Sensor Based on a Surface Acoustic Wave Resonator***
Feng Gao{2}, Amine Bermak{1}, Chi-Ying Tsui{2}, Farid Boussaid{3}
{1}Hamad Bin Khalifa University / Hong Kong University of Science and Technology, Qatar; {2}Hong Kong University of Science and Technology, Hong Kong; {3}University of Western Australia, Australia

15:51 ***A Low-Power 10-Bit Multichannel Analyzer Chip for Radiation Detection***
Joseph Schmitz, Mahir Gharzai, Sina Balkir, Michael Hoffman, Mark Bauer
University of Nebraska-Lincoln, United States

16:09 ***A Non-Invasive Material Sensing System and its Integrated Interface Circuits***
Yang-Jing Huang{2}, Heng-Ching Wu{2}, Po-Sheng Chen{2}, Hsu-Tao Shen{1}, Sheng-Yu Peng{2}, Chii-Wann Lin{1}
{1}National Taiwan University, Taiwan; {2}National Taiwan University of Science and Technology, Taiwan

16:27 ***CMOS Luminescence Lifetime Sensor for White LED Multi-Spectral Characterization***
Guoqing Fu, Sameer Sonkusale
Tufts University, United States

Modeling and Design Tools
Time: Wednesday, May 31
Room: Grand Ballroom X
Chair(s): Filippo Neri - u-blox, Switzerland; Nuno Paulino - UNINOVA

15:15 ***Processes of AM-PM Distortion in Large-Signal Single-FET Amplifiers***
Soheil Golara{1}, Shervin Moloudi{2}, Asad Abidi{3}
{1}Qualcomm Atheros Inc., United States; {2}Qualcomm Inc., United States; {3}University of California, Los Angeles, United States

15:33 ***INVITED: Weighted Kirchhoff Index of a Resistance Network and Generalization of Foster's Theorem***
Krishnaiyan Thulasiraman, Mamta Yadav
University of Oklahoma, United States

15:51 ***Formal Analysis of High-Performance Stabilized Active-Input Current Mirror***
Mohan Julien, Serge Bernard, Fabien Soulier, Vincent Kerzérho, Guy Cathébras
Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, France

16:09 ***Methodology for Automated Phase Noise Minimization in RF Circuit Interconnect Trees***
Dimo Martev{2}, Sven Hampel{1}, Ulf Schlichtmann{2}
{1}Intel Germany, Germany; {2}Technische Universität München, Germany

16:27 ***Analog Layout Retargeting with Process-Variation-Aware Rule-Based OPC***
Xuan Dong, Lihong Zhang
Memorial University of Newfoundland, Canada

Nanoelectronics I
Time: Wednesday, May 31 (15:15-16:45)
Room: Laurel AB
Chair(s): Robert Chen-Hao Chang - National Chung Hsing University/National Chi Nan University; Sorin Cotofana - Delft University of Technology

15:15 ***A SPICE Model of the Ta2O5/TaOx Bi-Layered RRAM***
Firas Hatem, Nandha Kumar, Haider Almurib
university of Nottingham Malaysia Campus, Malaysia

15:33 ***Record fT, fmax, and GHz Amplification in 2Dimensional CVD MoS2 Embedded Gate Fets***
Atresh Sanne{2}, Saungeun Park{2}, Rudresh Ghosh{2}, Maruthi Nagavalli Yogeesh{2}, Chison Liu{2}, Deji Akinwande{2}, Sanjay Banerjee{2}, Leo Mathew{1}, Rajesh Rao{1}
{1}Applied Novel Devices Inc., United States; {2}University of Texas at Austin, United States

15:51 ***High-Power Memristor Model and its Application***
Dongyuan Qiu, Bo Zhang, Yanfeng Chen, Yuehai Lu
South China University of Technology, China

16:09 ***Exploration and Evaluation of Low-Dropout Linear Voltage Regulator with FinFET, TFET and Hybrid TFET-FinFET Implementations***
Chia-Ning Chang, Yin-Nien Chen, Po-Tsang Huang, Pin Su, Ching-Te Chuang
National Chiao Tung University, Taiwan

16:27 ***A Small Area and Low Power True Random Number Generator Using Write Speed Variation of Oxide-Based RRAM for IoT Security Application***
Jianguo Yang, Yinyin Lin, Yarong Fu, Xiaoyong Xue, Ba Chen
Fudan University, China

Advanced Digital Techniques
Time: Wednesday, May 31 (15:15-16:45)
Room: Laurel CD
Chair(s): Izzet Kale - University of Westminster; Emre Salman - Stony Brook University

15:15 ***Time-Encoded Values for Highly Efficient Stochastic Circuits***
M. Hassan Najafi, Shiva Jamali-Zavareh, David Lilja, Marc Riedel, Kia Bazargan, Ramesh Harjani
University of Minnesota Twin Cities, United States

15:33 ***Sense Amplifier Half-Buffer (SAHB): a Low-Power High-Performance Asynchronous Logic QDI Cell Template***
Kwen-Siong Chong, Weng-Geng Ho, Tong Lin, Bah-Hwee Gwee, Joseph Sylvester Chang
Nanyang Technological University, Singapore

15:51 ***Design Methodology for Voltage-Scaled Clock Distribution Networks***
Can Sitik{1}, Weicheng Liu{2}, Baris Taskin{1}, Emre Salman{2}
{1}Drexel University, United States; {2}Stony Brook University, United States

16:09 ***Optimal Single Constant Multiplication Using Ternary Adders***
Martin Kumm{2}, Peter Zipf{2}, Oscar Gustafsson{1}, Mario Garrido{1}
{1}Linköping University, Sweden; {2}Universität Kassel, Germany

Future Technology for Circuits and Systems
Time: Wednesday, May 31 (15:15-16:45)
Room: Kent AB
Chair(s): Sorin Cotofana - Delft University of Technology; Yeong-Kang Lai - National Chung Hsing University

15:15 ***Eenergy and Delay Tradeoffs of Soft Error Masking for 16nm FinFET Logic Paths: Survey and Impact of Process Variation in Near Threshold Region***
Faris Alghareb{2}, Ahmad Alzahrani{2}, Ronald F. DeMara{2}, Rizwan Ashraf{1}
{1}Oak Ridge National Laboratory, United States; {2}University of Central Florida, United States

15:33 ***SPICE Compact Modeling of Bipolar/Unipolar Memristor Switching Governed by Electrical Thresholds***
Fernando García-Redondo{1}, Marisa López-Vallejo{1}, Robert Gowers{3}, Liudi Jiang{3}, Albert Crespo-Yepes{2}
{1}Universidad Politécnica de Madrid, Spain; {2}Universitat Autònoma de Barcelona, Spain; {3}University of Southampton, United Kingdom

15:51 ***Series-Parallel Charge Pump Conditioning Circuits for Electrostatic Kinetic Energy Harvesting***
Armine Karami{1}, Dimitri Galayko{1}, Philippe Basset{2}
{1}Laboratoire d'informatique de Paris 6 / Université Pierre et Marie Curie / Sorbonne Universités, France; {2}Université Paris-Est - ESIEE, France

16:09 ***Insights Into Tunnel FET-Based Charge-Pumps and Rectifiers for Energy Harvesting Applications***
Francesc Moll{2}, David Cavalheiro{2}, Stanimir Valtchev{1}
{1}Universidade Nova de Lisboa, Portugal; {2}Universitat Politècnica de Catalunya, Spain

16:27 ***Benchmarking TFET from a Circuit Level Perspective: Applications and Guideline***
Lingyi Guo, Le Ye, Cheng Chen, Qianqian Huang, Libo Yang, Zhu Lv, Xia An, Ru Huang
Peking University, China

IEEE International Symposium on Circuits & Systems
Conference Center, Florence, Italy, May 27-30, 2018

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FLOOR PLANS

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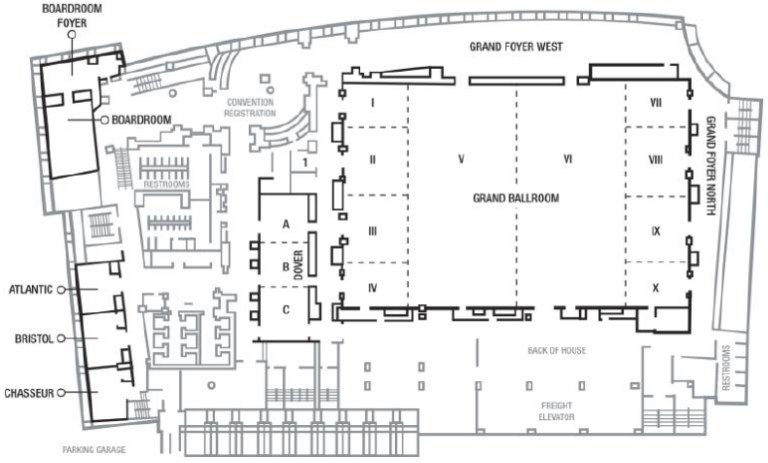
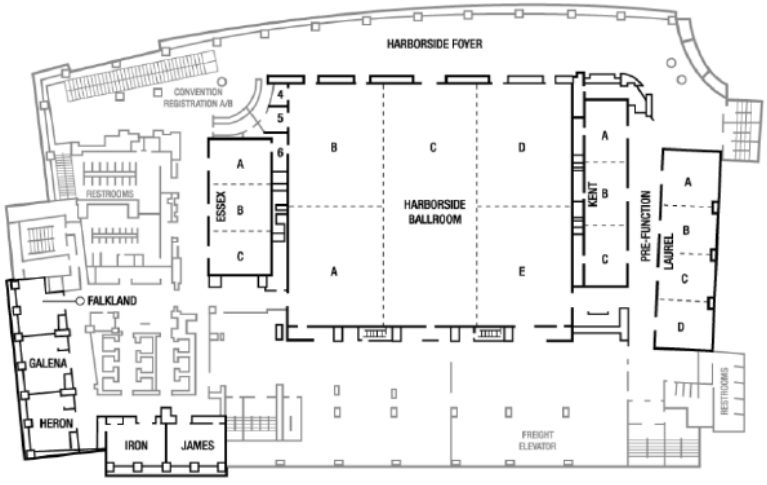


FOURTH FLOOR LEVEL



PROGRAM AT A GLANCE

Sunday May 28th

8:00 am – 6:00 pm | *ISCAS 2017 Conference registration*
9:00 am – 10:30 am | *Morning tutorials*
10:30 am – 11:00 am | *Break*
11:00 am – 12:30 pm | *Morning tutorials*

12:30 pm – 1:30 pm | *Lunch*

1:30 pm – 3:00 pm | *Afternoon tutorials*
3:00 pm – 3:30 pm | *Break*
3:30 pm – 5:00 pm | *Afternoon tutorials*
6:30 pm – 8:30 pm | *Welcome reception at Maryland Science Center*

Monday May 29th

8:00 am – 9:30 am | *Technical Sessions*
9:30 am – 11:00 am | *Welcoming remarks & Keynote Speaker*
11:00 am – 11:30 am | *Break*
11:30 am – 1:00 pm | *Technical Session*

1:00 pm – 2:00 pm | *Lunch*

2:00 pm – 3:30 pm | *Technical sessions*
2:00 pm – 5:00 pm | *Demo Session*
3:30 pm – 5:00 pm | *Poster Session*
5:00 pm – 6:00 pm | *Pioneers of CAS*
6:00 pm – 7:15 pm | *WiCAS Panel*
7:15 pm – 8:45 pm | *WiCAS/YP Reception*

Tuesday May 30th

8:00 am – 9:30 am | *Technical Sessions*
9:30 am – 10:30 am | *Keynote Speaker*
10:30 am – 11:00 am | *Break*
11:00 am – 12:30 pm | *Technical Session*

12:30 pm – 1:30 pm | *Lunch*

1:30 pm – 3:00 pm | *Technical Sessions*
1:30 pm – 4:30 pm | *Demo Session*
3:00 pm – 4:30 pm | *Poster Sessions*
4:30 pm – 5:30 pm | *Pioneers of CAS*
6:30 pm – 10:30 pm | *Conference Dinner at Ft. McHenry*

Wednesday May 31st

8:00 am – 9:30 am l *Technical Sessions*
9:30 am – 10:00 am l *Break*
10:00 am – 10:45 am l *Awards*
10:45 am – 11:45 am l *Keynote Speaker*

11:45 am – 1:30 pm l *Lunch*

1:30 pm – 3:00 pm l *Technical Sessions*
3:00 pm – 3:15 pm l *Break*
3:15 pm - 4:45 pm l *Technical Sessions*
5:30 pm – 7:30 pm l *Farewell Reception at Power Plant Live!*

AUTHOR INDEX